1989-12

Development and integration of the NPS middle ultraviolet spectrograph with an extreme ultraviolet spectrograph

Campbell, Richard S.

Monterey, California. Naval Postgraduate School

http://hdl.handle.net/10945/26983

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

DEVELOPMENT AND INTEGRATION OF THE NPS MIDDLE ULTRAVIOLET SPECTROGRAPH WITH AN EXTREME ULTRAVIOLET SPECTROGRAPH

by

Richard S. Campbell

December 1989

Thesis Co-Advisor: David D. Cleary
Co-Advisor: Sherif Michael

Approved for public release; distribution is unlimited.

UNCLASSIFIED
CURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

a REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b RESTRICTIVE MARKINGS
a SECURITY CLASSIFICATION AUTHORITY	3 DISTRIBUTION/AVAILABILITY OF REPORT APPROVED FOR PUBLIC RELEASE; DISTRIBUTION IS UNLIMITED.
b DECLASSIFICATION/DOWNGRADING SCHEDULE	
PERFORMING ORGANIZATION REPORT NUMBER(S)	5 MONITORING ORGANIZATION REPORT NUMBER(S)
a NAME OF PERFORMING ORGANIZATION NAVAL POSTGRADUATE SCHOOL 6b OFFICE SYMBOL (If applicable) 39	7a NAME OF MONITORING ORGANIZATION NAVAL POSTGRADUATE SCHOOL
c. ADDRESS (City, State, and ZIP Code) MONTEREY, CA 93943-5000	7b ADDRESS (City, State, and ZIP Code) MONTEREY, CA 93943-5000
8a NAME OF FUNDING/SPONSORING ORGANIZATION 8b OFFICE SYMBOL (If applicable)	9 PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State, and ZIP Code)	10 SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO / PROJECT NO / TASK NO / WORK UNIT ACCESSION NO

11 TITLE (Include Security Classification)
DEVELOPMENT AND INTEGRATION OF THE NPS MIDDLE ULTRAVIOLET SPECTROGRAPH WITH AN EXTREME ULTRAVIOLET SPECTROGRAPH

12 PERSONAL AUTHOR(S)
CAMPBELL, RICHARD S.

13a TYPE OF REPORT	13b TIME COVERED	14 DATE OF REPORT (Year, Month, Day)	15 PAGE COUNT
MASTER'S THESIS	FROM ________ TO ______	1989, DECEMBER	173

16 SUPPLEMENTARY NOTATION THE VIEWS EXPRESSED IN THIS THESIS ARE THOSE OF THE AUTHOR AND DO NOT REFLECT THE OFFICIAL POLICY OR POSITION OF THE DEPARTMENT OF DEFENSE OR THE U.S. GOVERNEMENT.

17 COSATI CODES			18 SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	EXTREME ULTRAVIOLET SPECTROGRAPH; MIDDLE ULTRAVIOLET SPECTROGRAPH; SOUNDING ROCKET EXPERIMENT

19 ABSTRACT (Continue on reverse if necessary and identify by block number)

CURRENT MEASUREMENTS OF IONOSPHERIC ELECTRON DENSITIES ARE ACCURATE BUT LIMITED IN SCOPE. PRESENT MEASUREMENT TECHNIQUES ARE LAND-BASED AND THE RESULTING DATA IS NOT GLOBAL IN NATURE. SCIENTISTS AT THE NAVAL POSTGRADUATE SCHOOL (NPS) AND THE NAVAL RESEARCH LABORATORY (NRL) ARE WORKING ON A JOINT RESEARCH PROJECT TO DEVELOP A TECHNIQUE TO DETERMINE GLOBAL IONOSPHERIC ELECTRON DENSITIES FROM SATELLITE PLATFORMS. NPS DEVELOPED A MIDDLE ULTRAVIOLET SPECTROGRAPH WITH WAVELENGTH COVERAGE OF 1800 TO 3400 Å. THIS THESIS DEVELOPED THE INTEGRATION PACKAGE THAT LINKED THE SPECTROGRAPH ANALOG DATA TO THE AYDIN VECTOR MMP-600 PCM ENCODER. THE INTEGRATION PACKAGE PROVIDED ANALOG-TO-DIGITAL CONVERSION OF THE DATA, DATA STORAGE FOR THE DIGITAL

20 DISTRIBUTION/AVAILABILITY OF ABSTRACT ☒ UNCLASSIFIED/UNLIMITED ☐ SAME AS RPT ☐ DTIC USERS	21 ABSTRACT SECURITY CLASSIFICATION UNCLASSIFIED
22a NAME OF RESPONSIBLE INDIVIDUAL DR. DAVID D. CLEARY	22b TELEPHONE (Include Area Code) (408) 646-2828 22c. OFFICE SYMBOL 61 Cl

DD Form 1473, JUN 86 Previous editions are obsolete. SECURITY CLASSIFICATION OF THIS PAGE

S/N 0102-LF-014-6603 UNCLASSIFIED

LINE #19 (CONT.)

DATA, AND SYNCHRONIZATION OF THE DATA COLLECTION AND DATA TRANSMISSION OPERATIONS. TESTING EQUIPMENT WAS ALSO DEVELOPED TO SUPPORT LABORATORY CALIBRATION AND IN-PLACE TESTING OF THE INSTRUMENT. THE TEST EQUIPMENT PROVIDES COMPUTER GENERATED SYNCHRONIZATION SIGNALS AND DIGITAL DATA ACQUISITION.

Approved for public release; distribution is unlimited.

DEVELOPMENT AND INTEGRATION OF THE NPS MIDDLE ULTRAVIOLET SPECTROGRAPH WITH AN EXTREME ULTRAVIOLET SPECTROGRAPH

by

Richard S. Campbell
Lieutenant, United States Navy
B.S.E.E., United States Naval Academy, 1980

Submitted in partial fulfillment
of the requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
December 1989

ABSTRACT

Current measurements of ionospheric electron densities are accurate but limited in scope. Present measurement techniques are land-based and the resulting data is not global in nature. Scientists at the Naval Postgraduate School (NPS) and the Naval Research Laboratory (NRL) are working on a joint research project to develop a technique to determine global ionospheric electron densities from satellite platforms. NPS developed a middle ultraviolet spectrograph with wavelength coverage of 1800 to 3400 Å. This thesis developed the integration package that linked the spectrograph analog data to the Aydin Vector MMP-600 PCM Encoder. The integration package provided analog-to-digital conversion of the data, data storage for the digital data, and synchronization of the data collection and data transmission operations. Testing equipment was also developed to support laboratory calibration and in-place testing of the instrument. The test equipment provides computer generated synchronization signals and digital data acquisition.

TABLE OF CONTENTS

ACKNOWLEDGEMENT

The general involvement in this thesis is symbolic of the genuine dedication embodied by the majority of the people associated with government research. Initially, I would like to thank Harry Merchant for his continual support and patience as he single-handedly schooled me on the intricacies of applied electronics and their applications to rocket experiments. More importantly, Harry provided encouragement and support when project complications seemed insurmountable. Without his guidance, I am sure the project would not have achieved the success that it ultimately did.

I am indebted to Dave Rigmaiden for his hours of technical support in the areas of circuit board fabrication, flight grade electronics assembly, and artwork fabrication for circuit board etching. Dale Galarowicz assembled the flight instrument and, in my estimation, was the only person at the school with the technical experience to perform this task. George Jaksha and Steve Blankschein professionally machined the test and flight chassis to support the instrument development.

Dr. David Cleary provided the topic and the dedicated assistance to ensure the successful completion of the project. His patience and sense of humor in view of the projects numerous failures and setbacks was commendable. Furthermore,

his far reaching connections and acquaintances were invaluable resources in the search for components and guidance.

Both Dr. Cleary and Dr. Sherif Michael must be commended on their unfaltering support and assistance in the writing of this paper.

Finally, I would like to thank my wife and family for living with this thesis as well as myself for the last nine months. On numerous occasions I was inattentive to the needs of my family and through it all they were always supportive of the project.

I. INTRODUCTION [Ref. 1]

On March 21, 1986, the Joint Chiefs of Staff issued a memorandum (MJCS 154-86) which listed the prioritization of research requirements for defense environmental satellites. Measurement of the electron density of the Earth's ionosphere ranked fifth on this list of fifty requirements. Knowledge of ionospheric electron density is essential for the development of many high frequency (HF) military systems. Ongoing research is presently being conducted in the following areas:

- HF radio communications
- Over-The-Horizon (OTH) radar
- Ballistic Missile Early Warning System (BMEWS)
- Ground Wave Emergency Network (GWEN).

The above-mentioned systems all require an in-depth knowledge of global electron densities, as these systems rely on the ionosphere's ability to reflect and bend HF electromagnetic waves. Current measurements of the ionospheric electron densities are accurate but limited in scope. Measurements are obtained from either ground-based radar stations or ionosonde stations. Presently, twenty ionosonde stations located primarily in North America provide limited electron density data. Current data is not global in nature and to obtain

global data with current operational systems is economically and politically unfeasible.

Satellites provide one method to measure global electron densities. Satellite-based ionosondes (topside sounders) are impractical due to large size and power requirements. Although active sensing is technically prohibitive, space-based systems have successfully employed energy and weight efficient passive techniques. Scientists at the Naval Research Laboratory (NRL) are investigating a passive technique for inferring electron densities in the F2 region of the ionosphere by measuring the O^+ emissions at a wavelength 834 Å (1 Å = 10^{-10} meters). The measurement is expected to provide accurate data above an altitude of 200 km.

Below the altitude of 200 km, O_2^+ and NO^+ become the dominant ions in the regions known as the D-, E-, and F1-layers. The Naval Postgraduate School (NPS) is investigating a method for inferring the electron densities at altitudes below 200 km. The technique involves the measurement of the neutral species N_2, O_2, O, NO, and N. Photochemical models of the ionosphere have shown that these neutral species are chemically coupled with O_2^+ and NO^+. The E-region electron density can be accurately inferred from a knowledge of the neutral species density.

Dedicated research at both NRL and NPS has resulted in the approval of a National Aeronautics and Space Administration (NASA) rocket experiment (36.053E). The launch is scheduled

for February 1990 at White Sands Missile Range in New Mexico. Using a two-stage Terrier-Black Brant launch vehicle, the rocket is expected to reach a maximum altitude of 350 km. Two instruments will be flown on the experiment. The NRL-sponsored instrument, named HIRAAS, is a 0.5 m Rowland Circle Spectrograph with wavelength coverage of 500 Å to 1500 Å. The NPS-sponsored instrument, named MUSTANG, is a middle ultraviolet spectrograph with wavelength coverage of 1800Å to 3400 Å. The spectrograph is a 1/8 m Ebert-Fastie with a micro-channel plate (MCP) image intensifier and a 512 linear array detector. The instruments will obtain data between the altitude of 100 and 350 km. Data from the NPS MUSTANG experiment will be telemetered to the ground station. The NRL HIRAAS instrument will record its data on electrographic film which will be recovered at completion of the flight.

The development and integration of MUSTANG required close interfacing with NRL, NASA (Goddard Space Center), and Research Support Instruments (RSI-instrument construction). Figure 1.1 illustrates the integrated MUSTANG/HIRAAS experiment positioned in the payload section of the launch vehicle. The evolution of Mustang into an integrated flight experiment is documented in Chapters II-V of this thesis.

Chapter II discusses the operational characteristics of the NASA provided telemetry package and the RSI detector and support components.

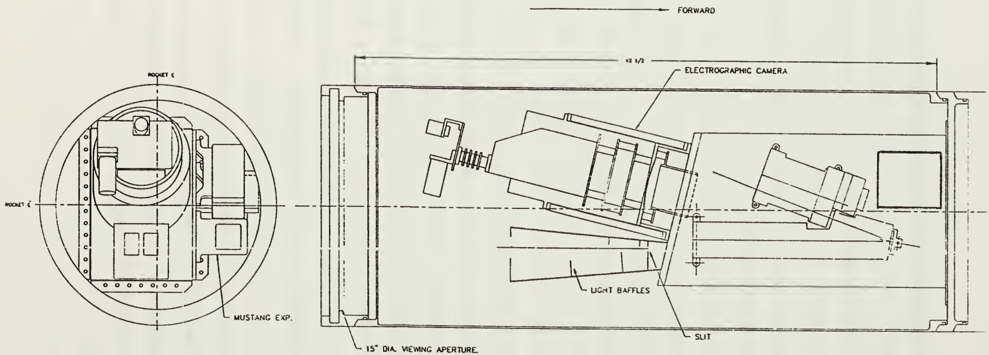


Figure 1.1 Integrated MUSTANG/HIRAAS Payload [Ref. 2]

Chapter III discusses the design interface required to couple the detector to the telemetry package.

Chapter IV discusses bench check equipment (BCE) interfacing and development.

Chapter V discusses interface board fabrication, construction, integration and testing.

Chapter VI presents conclusions and recommendations for future projects.

II. DESIGN CHARACTERISTICS OF MANUFACTURED FLIGHT COMPONENTS

MUSTANG development is based on modular construction ensuring a cost-effective/flexible instrument that can be operated in a variety of experimental environments. Currently, the instrument is configured to operate within the constraints of the sounding rocket experiment. With minor modifications, the instrument could be fitted to a space shuttle experiment or the instrument could be utilized in support of a laboratory experiment. The MUSTANG electronics can be divided into four subsystems: the detector, the interface board, the power supplies, and the PCM encoder (see Figure 2.1). All the subsystems, with the exception of the interface board, will be described in this chapter. Chapter III will consider the design requirements of the interface board.

A. PCM ENCODER SUBSYSTEM [Ref. 3]

1. Configuration

The PCM encoder has flown on more than 70 sounding rockets without an in-flight anomaly. The encoder utilizes the Aydin Vector MMP-600 Series micro-miniature PCM system. Characteristics of the system include small size (light), low power consumption, and programmable flexibility. Designed as a modular system, the encoder allows for a variety of configurations to meet the control and data dissemination

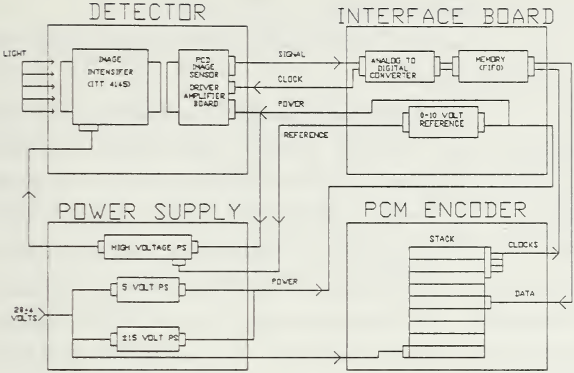


Figure 2.1 Block Diagram of Mustang Subsystems

requirements of the experiment. Each encoder "stack" consists of two groups of modules. A typical PCM stack is shown in Figure 2.2. Group I modules are required for all configurations. Group II modules are selected based on the requirements of the experiment.

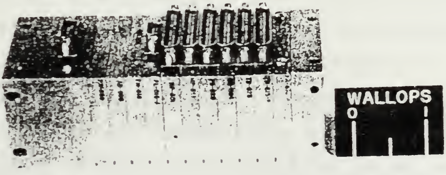


Figure 2.2 Example of PCM Stack [Ref. 3:p. 2]

a. Group I Modules

One each of the modules listed below are required in every PCM system.

(1) **PX-628 Power Supply**. The power supply module requires a source voltage of 28 ± 4 v and provides regulated 28 v to the remainder of the PCM encoder system. The system oscillator is located inside the power supply module. Selection of the oscillator frequency is accomplished by manipulating a set of jumpers found on the external connector of the module. For this experiment, the oscillator frequency is set to 200 kbits/sec ensuring that the maximum clockrate of the detector (250 kHz) is not exceeded. The bit clock is a 0 to +5 v pulse train that is CMOS- and low power TTL-compatible.

(2) **PR-614 Programmer**. The programmer module houses the control circuit. The programmer executes the software program that has been entered into the 256x8 erasable programmable read-only memory (EPROM) and controls the timing and operation of the entire system. MUSTANG utilizes the timing control of the PCM encoder to synchronize its operation (more thoroughly discussed in Chapter III).

(3) **FM-618 Formatter**. The formatter module, controlled by the programmer, takes digitized data and merges it with frame synchronization words. The data undergoes parallel to serial conversion to provide the proper data format for the timer.

(4) **TM-615P Timer**. The timer module accepts serial data from the formatter and encodes this data into the required PCM data format (Bi-0-L). The data format is selected by setting jumpers located on the external input connector. Word format is also selectable on the input connector and is currently selected to 10 bits/word. Interfacing the encoder timing signals to external circuits is accomplished by utilizing an external output connector. The following output signals may be accessed:

- NRZ-L output
- Bi-0-L output
- NRZ-L primary output
- Major Frame synchronization
- Bi-0-L primary output
- Premodulation filter output
- Inverted 2x bit clock(0-10v)
- 2x bit clock
- Bi-0/NRZ, mark/space coded output
- Inverted Bi-0/NRZ, mark/space coded output
- Inverted bit clock
- Minor frame synchronization
- Word clock
- Bit clock.

(5) **EP-612 End Plate**. The end plate terminates the PCM stack on the end opposite the power supply. The EPROM is housed inside the module and access is obtained through a

removable cover. The EPROM is socketted (contrary to the standard practice of soldering) to allow for EPROM reuse.

b. Group II Modules

Group II modules are optional and are added to support the unique data requirements of the experiment. The modules listed below either support MUSTANG uniquely or support MUSTANG and HIRAAS collectively.

(1) <u>PD-629 Digital Parallel Multiplexer with Two Enables</u>. The PD-629 module has the capability of accepting three independent channels of parallel words consisting of 10 bits/word. The multiplexer is controlled by the program loaded into the EPROM. The experiment will fly two modules allowing for the direct integration of six channels of digital data. MUSTANG will exclusively utilize one channel for the transmission of experimental data. The remainder of the channels will be utilized for programmed events not associated with MUSTANG. Each module is referenced with an unique address that is recognized by the EPROM. The address is programmed by setting jumpers located on the external input connector of the module. Two of three input channels (10 parallel bits/channel) on the module have an external enable associated with them. The enable pulse may be used to signal external circuits that parallel data on the respective channel is being accessed. The importance of the enable pulse, relative to MUSTANG, will be addressed in Chapter III.

(2) **MP-601L 32-Channel High-Level Analog Multiplexer**. The analog multiplexer accepts 32 channels of analog data with inputs limited from 0 to +5.0 v. The experiment will fly three modules to process the 96 channels of required analog data every 51.2 msec. To satisfy the Nyquist criteria each channel will be limited to a bandwidth of 9.7 Hz. MUSTANG will utilize three channels of analog data to provide monitoring of the 5 v, $\pm$15 v, and high volt busses. The majority of the analog signals are used for monitoring various rocket parameters and control signals. Control of the multiplexer is determined by the EPROM program. Each module is programmed with an unique address by setting jumpers found on the external connector.

(3) **AD-606-HS Analog-to-Digital Converter (ADC) with Sample and Hold**. The AD-606-HS module digitizes the analog data requiring transmission. The signal input to the module is the EPROM-controlled output of one of the three analog multiplexers mentioned above. Again, the input signal is limited to a voltage range of 0 to +5.0 v. The analog-to-digital converter digitizes each analog signal into a ten-bit binary word utilizing the method of successive approximation. At the completion of digitizing, the digital signal is sent to the formatter for inclusion into the programmed PCM encoder matrix.

(4) **FL-619A Quad Filter and Amplifier**. The quad filter module provides linear-phase lowpass premodulation

filtering of the serial output from the timer module. Each filter module contains four independent filters which share a common lead with the input signal from the unfiltered output of the timer module. Filter selection is achieved by choosing the respective output of the desired filter. The -3dB upper cutoff frequency for Bi-ϕ-L coding is determined by the following formula:

$$1.4 \times \text{bitrate} = \text{upper cutoff frequency} \tag{1.1}$$

$$1.4 \times 200 \text{ kbits/sec} = 280 \text{ kHz.} \tag{1.2}$$

Based on the above calculation, the 280 kHz lowpass filter was chosen for this experiment. A signal gain adjustment at the filter output allows for the accurate integration of the PCM encoder with the rocket's transmitter (specifically the modulator). Figure 2.3 illustrates the "stack" position of each PCM encoder module as required by the experiment.

2. Operation

Operation of the PCM encoder is implied from the discussion of the system component parts. Figure 2.4 provides a basic block diagram of the PCM encoder that will be utilized for the experiment. Data for the experiment comes in two forms, analog or digital. Analog data must be synchronized and digitized prior to formatting. The analog data synchronization is controlled by the processor (PR-614) operating under a software program loaded into the system

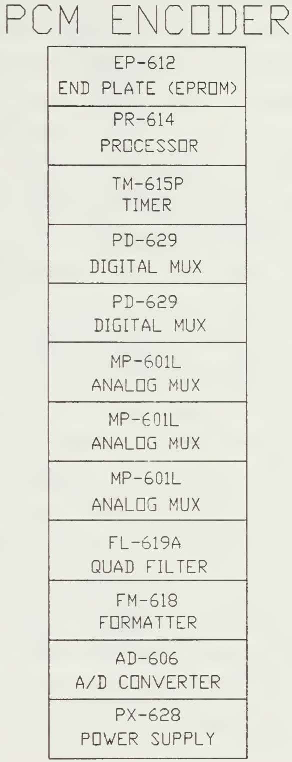


Figure 2.3 Flight Configured PCM Encoder Stack
[After Ref. 3:p. 4]

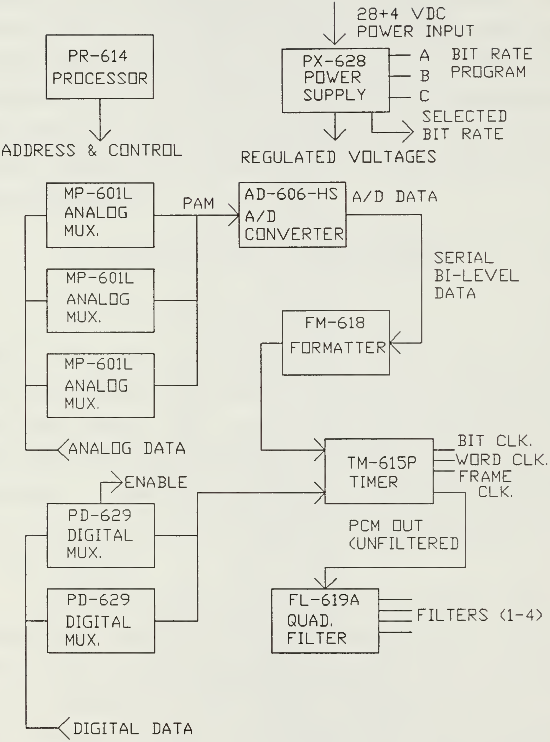


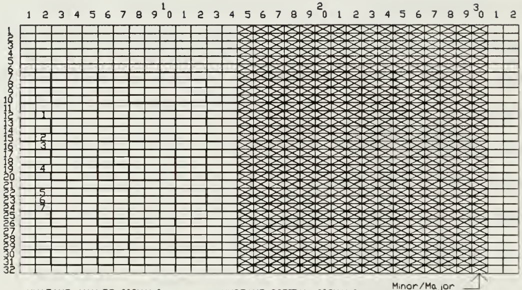
Figure 2.4 Flight Configured PCM Encoder Block Diagram
[After Ref. 3:p. 5]

EPROM. Synchronization occurs at the analog multiplexers (MP-601L) and the data is accessed at the output of the analog to digital converter when the formatter (FM-618) is instructed to access the data. Digital data is synchronized at the digital multiplexers and is accessed by the formatter when instructed to do so. Data entering the formatter is in a parallel format. The formatter does a parallel-to-serial conversion on all data and merges the synchronization words into the PCM word format. The timer module (TM-615P) accepts the serial data, encodes the bitstream into Bi-0-L format, and provides an unfiltered output to the quad filter (FL-619A). The quad filter provides lowpass filtering and gain adjustment prior to modulation in the transmitter. The PCM-encoded format, showing the word location of MUSTANG's experimental data, is illustrated in Figure 2.5 [Ref. 4].

The telemetry system utilizes a 200 kbit/sec PCM/FM RF link at a carrier frequency of 2269.5 MHz. The transmitter is a 5 watt Vector T105. A bit error probability of 10^{-6} is achieved given that the signal-to-noise ratio for the PCM/FM system is 13 dB (value provided by Aydin Vector). Utilizing the manufacturer's data and NASA's receiving station data, a link margin of 13.7 dB was calculated. [Ref. 4]

3. Signals

Reference signals generated by the PCM encoder are utilized by MUSTANG to ensure synchronized data collection, processing, and dissemination. Figure 2.6 illustrates the



MUATANG ANALOG SIGNALS

1. Experimental high voltage
2. ±15V DC/DC monitor
3. 5V DC/DC monitor
4. 28V battery monitor
5. 5V amplifier monitor
6. 15V amplifier monitor
7. 5v high voltage monitor

MUSTANG DIGITAL SIGNALS

X Experimental data

Minor/Major Sync Frames

Bit clock frequency is..........200 kHz (5usec/bit)
Each word consists of..........10 bits/word (50usec/word)
Each frame consists of..........10,240 bits/frame
..........1,240 words/frame
Each frame..........51.2 msec/frame
Each minor frame..........1.6 msec/subframe

Figure 2.5 PCM Communication Matrix [After Ref. 3:p. A-1]

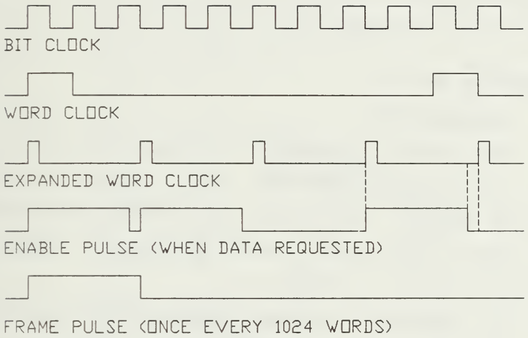


Figure 2.6 Timing Diagram Illustrating Flight Synchronization Signals [After Ref. 3:p. 43]

reference signals utilized by MUSTANG and the relative timing of each signal. Figure 2.4 illustrates the source of each signal. The reference signals generated by the PCM encoder combined with the reference signals generated by the detector (discussed below in Section B) provide the design basis for the interface board which will couple the detector to the PCM encoder (topic of Chapter III).

B. DETECTOR [Ref. 5]

1. Configuration

The MUSTANG instrument electronics consists of an image intensifier, a detector, and a low-noise driver amplifier circuit. The detector is a Plasma-Coupled Device (PCD) linear image sensor. A detailed mechanical diagram of MUSTANG is presented in Figure 2.7.

a. Hamamatsu PCD Linear Image Sensor (S-2300-512F)

The PCD linear image sensor is a monolithic (single crystal) integrated circuit which makes use of the coupling occurring in bulk silicon by virtue of the existence or non-existence of the plasma state of holes and electrons. The linear image sensor is composed of the photodiode, switching (output), and digital shift register sections. The PCD linear image sensor equivalent circuit is shown in Figure 2.8.

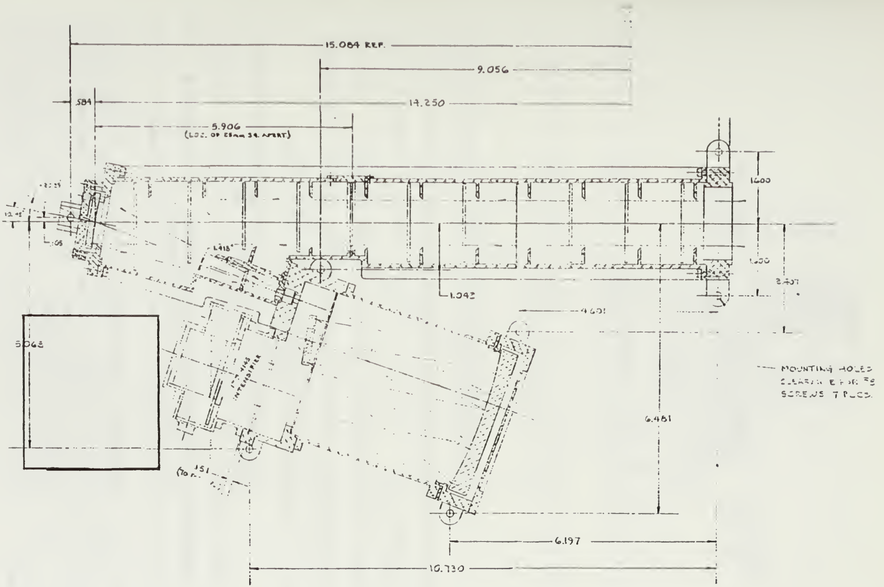


Figure 2.7 Mechanical Drawing of Mustang [Ref. 6]

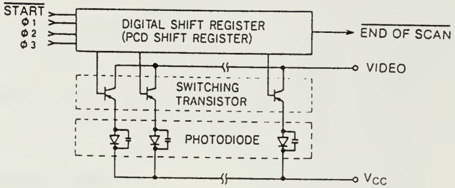


Figure 2.8 PCD Linear Image Sensor Equivalent Circuit [Ref. 5:p. 1]

(1) **Photodiode Section**. The light-sensitive section consists of 512 p-n junction photodiodes which perform both photoelectric conversion and charge storage. The photodiodes are designed to have low dark current. This is due to the buildup of charge when no photon source is present. Figure 2.9 illustrates the photodiode construction.

The photoelectric conversion characteristic of a light detector is determined by the ratio of incident light intensity to output signal level. To improve the performance of the detector in low light environments, it is desirable to integrate the output over time rather than observing the output directly. The PCD image sensors make use of the integration process to improve low light performance. Figure 2.10 illustrates the photoelectric

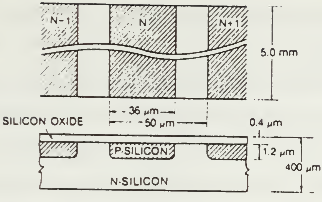


Figure 2.9 Geometry of Image Sensor Light Sensitive Section [Ref. 5:p. 14]

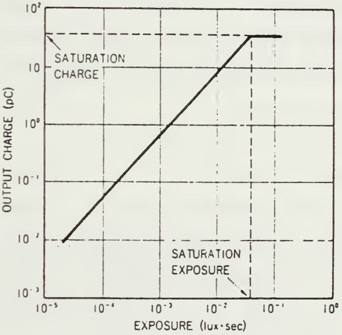


Figure 2.10 Image Sensor Photoelectric Conversion Characteristics [Ref. 5:p. 8]

conversion characteristics of the PCD image sensor. The incident exposure at the breakpoint of the linear portion of the curve represents the saturation exposure. The output

charge at saturation is dependent on the junction capacitance of the photodiodes.

The spectral response of the PCD image sensor is a measure of the output response with respect to input wavelength. The use of p-well construction limits the sensitivity in the long-wavelength regions and centers the maximum-sensitivity wavelength at 6000 Å. The reduction in long-wavelength sensitivity reduces the crosstalk between adjacent sensor elements. Figure 2.11 illustrates the spectral response of the PCD image sensor. MUSTANG utilizes a fiber optic window resulting in greater light rejection at the sensor input when compared to the observed response when the quartz window is used.

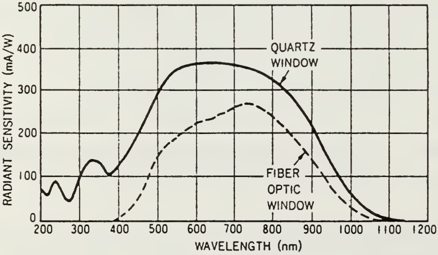


Figure 2.11 Spectral Response of the Image Sensor [Ref. 5:p. 8]

Image sensor resolution pertains to the ability of the sensor to reproduce the details of an observation. Since the photodiodes are mutually separated, sampling theory can be applied to the relationship between incident illumination and diode spacing. The light illumination can be no more than half the spacing between adjacent photodiodes. The resolution of the PCD image sensor is also dependent upon the input light wavelength. As wavelength increases, the photoelectric conversion takes place deeper within the silicon substrate and as the carriers travel toward the surface of the substrate, diffusion occurs which allows for the leakage of photons into adjacent sensors (see Figures 2.12 and 2.13).

A phenomenon, known as lag, occurs when the output of the current scan is affected by residual charge from a previous scan. Lag presents itself when rapidly-changing incident light exceeds the sensor's capability to follow such changes. Under static light conditions and when such rapid changes of intensity do not occur, negligible lag exists.

The presence of measurable image sensor output with no illumination is referred to as dark output. Dark output is always present and causes a reduction in the signal-to-noise ratio of the image sensor. Two types of phenomena generate dark output. In the photodiode region, dark output is a function of photodiode leakage current and integration (storage) time. The photodiode dark current is

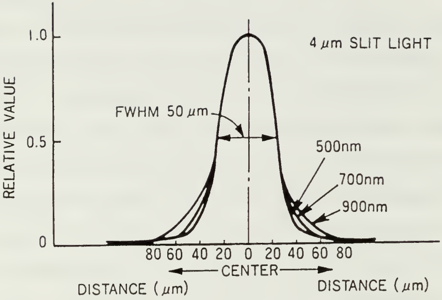


Figure 2.12 Leakage of Photocarriers into Adjacent Pixels [Ref. 5:p. 7]

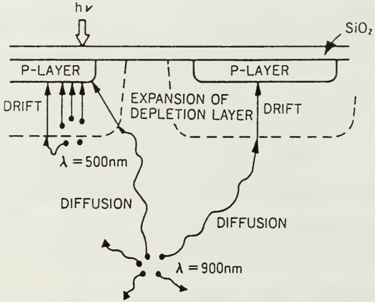


Figure 2.13 Conceptual Representation of Wave Length Impact on Diffusion [Ref. 5:p. 7]

very sensitive to temperature, doubling with each 7°C rise in temperature (see Figure 2.14). Dark output is also a function of PCD shift register leakage current and the signal readout time for each element. For long storage periods, dark output is dominated by photodiode leakage current. The greater the integration period, the smaller the dynamic range of the image sensor. As the storage time is reduced, leakage current from the shift register becomes dominant. The linear region of Figure 2.14 illustrates the dominance of the photodiode leakage current and the nonlinear region of the figure illustrates the dominance of the shift register leakage current.

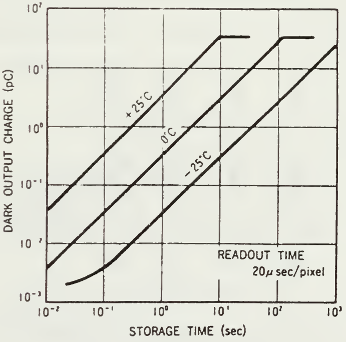


Figure 2.14 Dark Out Put Charge versus Storage Time Temperature Dependency [Ref. 5:p. 8]

(2) <u>**PCD Shift Register Section**</u>. The PCD transfer section is a digital shift register utilizing hooked conductance transistors (HCDT's) which are sharp current-controlled bistable switching elements with good on/off isolation. These elements are aligned in a row along the silicon substrate and they make use of the electrical coupling within the semiconductor. Figure 2.15 illustrates the transfer section equivalent circuit. The PCD shift register consists of a common anode and independent cathodes. If a discharge between a given anode and cathode occurs, the plasma existing between these two electrodes will impact the area around the adjacent cathode, reducing the discharge threshold voltage. By externally controlling the cathode voltage using a pulse input, it is possible to transfer a glow discharge

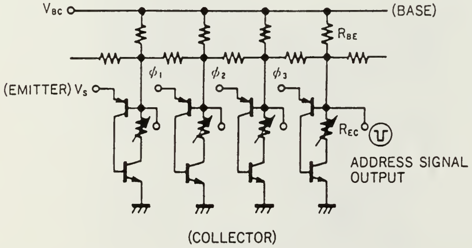


Figure 2.15 PCD Shift Register Equivalent Circuit [Ref. 5:p. 1]

from one cathode area to the adjacent cathode. The semiconductor implementation of this transfer method does not require wiring and is the essential operating principal behind the fast switching capability PCD shift register.

The HCDT's are separated from each other by a maximum of one carrier diffusion length. The register consists of an equivalent base, and independent emitters and collectors. When V_{BC} and V_E is applied, the current that flows between the emitters and the collectors exhibit current-control negative resistance characteristics. (Figure 2.16 shows the equivalent circuit for a single HCDT.) The voltage V_P, where the negative-resistance region begins, corresponds to the HCDT on voltage. If the HCDT is on, the semiconductor plasma occurring due to carrier accumulation will affect the adjacent collector region, lowering the threshold of the on

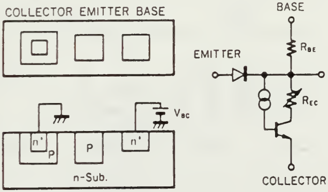


Figure 2.16 HCDT Equivalent Circuit [Ref. 5:p. 1]

voltage. By injecting a controlling current during this period it is possible to transfer the on-state to the adjacent HCDT. A three-phase clock will be the source of the controlling current. Clock selection for detector operation must be considered carefully. If the clock pulse amplitude is too high, the PCD shift register will saturate, rendering the output useless (i.e., all light collection circuits will discharge simultaneously). Likewise, if the clock pulse amplitudes are below the minimum threshold, the glow discharge will not transfer to the adjacent cathode. The variation between the maximum and minimum pulse level is referred to as the operating margin.

To ensure stable PCD shift register operation, the driver circuit of Figure 2.17 is utilized. The emitter resistance, $R_E=R_1+R_2$, and the emitter capacitance, C_E, impact the circuit operating characteristics by promoting

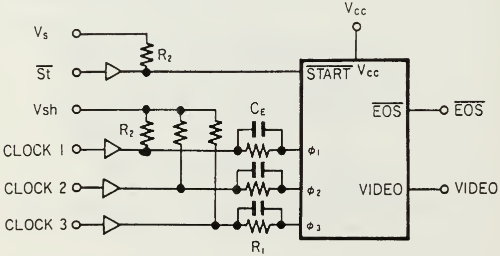


Figure 2.17 Clock Driver Circuit [Ref. 5:p. 2]

temperature stability and efficient power utilization. At high frequencies (>250 kHz), the R_1/C_E pair is removed to allow for stable clocking. In this case efficiency and stability are sacrificed for speed.

(3) <u>Switching (Output) Section</u>. The output section consists of a bank of lateral pnp switching transistors (refer to Figures 2.8 and 2.18 for implementation and equivalent circuit). The video signal (output) is generated when the PCD shift register sequentially addresses successive switching transistors allowing the photodiodes to discharge through the transistor collector, effectively transforming spatial data into a series of signals. The collectors of all switching transistors are tied to a common video line and the output data becomes available for collection at this point.

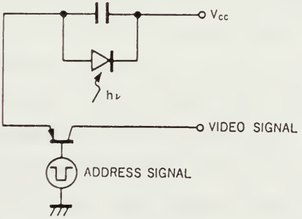


Figure 2.18 Switch Section Equivalent Circuit [Ref. 5:p. 1]

Two methods of data collection are possible. The current-detection method of data collection uses a resistive load tied to the video line. If the current-detection method is used, the data will be represented by a differentiated waveform. The output signal will be nonlinear with respect to the input signal and signal processing must be performed on the peak value of the wave form. The peak value will have a time variation dependent on the output level. If linear response or high accuracy at low output levels is required, the current-integration method of detection should be used. The integration method uses a charge amplifier to integrate the total output signal providing a rectangular wave shape which is easy to acquire and analyze. The process of integration ensures linear response by eliminating the time variation in the output signal (i.e., the variation averages out).

b. Hamamatsu Low Noise Driver/Amplifier Circuit

Hamamatsu provides a driver/amplifier circuit with a variety of useful control functions as illustrated in Figure 2.19. The amplifier board provides the control signal generation, the PCD clock driver required for stable switching, and the charge amplifier required for signal processing. The circuit is designed for interfacing with the very sensitive image sensor and proper filtering of power supplies results in low-noise operation (2700 electrons rms). The driver/amplifier circuit requires only five inputs to

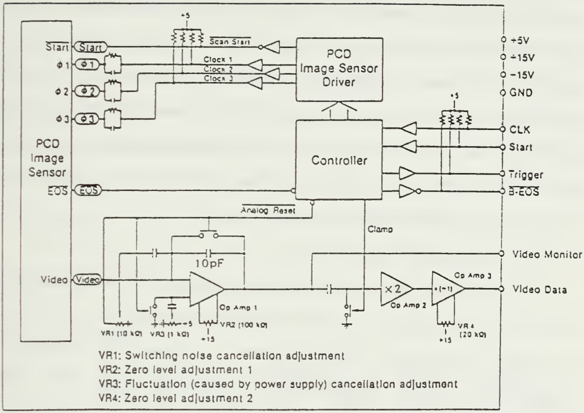


Figure 2.19 Block Diagram of Flight Qualified Driver Amplifier [Ref. 5:p. 9]

control and operate the image sensor, thereby reducing the complexity of user interface with the image sensor. The required inputs will be more fully discussed in the section on detector signals.

c. ITT Image Intensifier (F4145) [Ref. 7]

The image intensifier provides the mechanism for coupling the low level ultraviolet radiation (1800-3400 Å) to the PCD image sensor. Initially, the image intensifier accepts UV photons through a fiber optic window. Electrons are produced when the photons enter the photocathode. The

electrons pass through two microchannel plates in cascade under the influence of high voltage resulting in highly energetic electrons. The electrons are absorbed by a P-20 phosphor screen producing visible light over a visible spectrum of 4750-6000 Å. The high voltage can be controlled through the use of a reference voltage which is variable on the range 0-10 v. Adjusting the reference voltage to 10 v will provide the maximum gain ($4x10^4$)

2. **Detector Operation**

Through the use of optics, the MUSTANG spectrograph produces a spectrum over the desired wavelengths (1800-3400 Å at the instrument focal plane). These UV photons are converted (image intensifier) into an electron stream, accelerated, and reconverted into high energy photons at the wavelengths (4750-6000 Å) required for image sensor operation. The process of photon capture will continuously illuminate the PCD image sensor. The image sensor output is controlled through the application of a system clock and a start clock. The system clock provides the reference for the three-phase clock generated by the driver amplifier circuit. The start clock provides the start reference for data output. The frequency of the start clock will determine the integration period; the greater the clock frequency, the shorter the integration period.

3. Detector Signals

For synchronized operation, the detector requires two input reference signals, the system clock and a reference start clock. Two external reference signals are generated by the detector to synchronize the two channels of available data with the signal processing circuits. Figure 2.20 illustrates the relative relationship of the control and serial analog output signals. All signals are referenced to the system clock. The system clock will operate at the same frequency as the PCM encoder bit clock illustrated above in Figure 2.6.

C. POWER SUPPLIES

The rocket power system is composed of three independent 28 v unregulated busses (28±4 v). The three power busses consist of the instrumentation power system, the experiment power system, and the door power system. MUSTANG utilizes power from the experiment power system to provide analog and digital power to the detector and the interface board. The PCM encoder and Aydin Vector transmitter receive power from the instrumentation power system. The door power system provides the power to open the hermetically-sealed experiment door after rocket motor separation and provides power to the film advance motors utilized in the HIRAAS experiment. The door power system is separated from the electronic busses to ensure isolation of the motor-generated noise. A block diagram of the power distribution is illustrated in Figure 2.21. Each component requiring power must provide individual

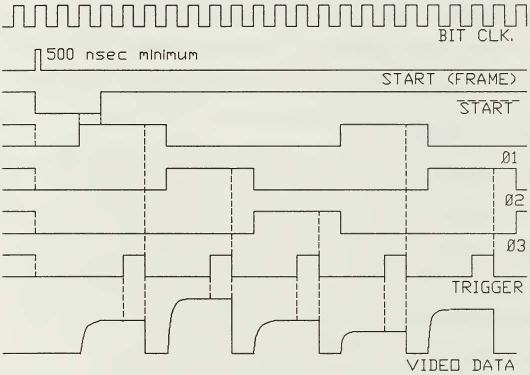


Figure 2.20 PCD Image Sensor Control And Data Signals [Ref. 5:p. 13]

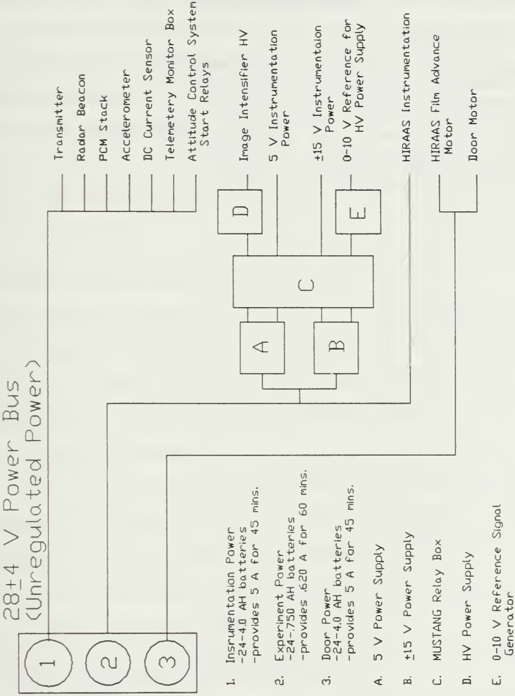


Figure 2.21 Block Diagram of the Power Supply

power regulation if the unregulated bus specifications exceed the limitations of the component. As mentioned previously, the PCM encoder and the data transmitter will accept unregulated 28 v dc power. The remainder of the MUSTANG power requirements will be provided by a 5 v regulator (digital power), a $\pm$15 v regulator (analog power), and a high voltage regulator (image intensifier power).

III. INTERFACE DESIGN

In Chapter II, The subsystems that provide data acquisition and control were presented. These subsystems have demonstrated operational reliability. The focus of this chapter is the design requirements of the interface circuit that couples MUSTANG to the sounding rocket telemetry and control subsystems.

A. CIRCUIT DESIGN REQUIREMENTS

The interface design requirement can be simply stated: given the analog output of the image sensor, design a system that will reformat and store the image sensor data until requested by the PCM encoder for transmission.

1. Signal Processing

The interface board must sample the analog serial data generated by the image sensor and format the data so that it is compatible with the PCM encoder. Three interface alternatives were considered, two of which were feasible. The alternatives considered were:

- Direct analog-to-digital (AD) conversion of the analog signal performed by the PCM encoder.
- Sample and hold the significant elements of the analog signal followed by AD conversion of the sampled data.
- Direct AD conversion of the significant elements of the analog signal by an independent analog-to-digital converter (ADC).

The physical positioning of the various rocket components (see Figure 3.1) precluded coupling the MUSTANG detector directly to the PCM encoder with the analog signal lead for three reasons:

- There is significant signal attenuation since the signal path is approximately five feet long.
- The signal lead would be forced to travel adjacent to inherently noisy systems such as the film-advance motor (used in HIRAAS), various power supplies, and the attitude control system.
- Given the data acquisition rate (Figure 2.20) and the telemetry requirements (Figure 2.5), it is operationally impossible to synchronize the generated analog signals to the operational requirements of the PCM ADC.

The second alternative, sampling the analog signal at the appropriate time and performing the subsequent AD conversion on the sampled signal, looked promising. The

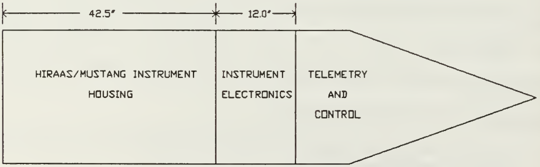


Figure 3.1 Sounding Rocket Configuration Block Diagram

leading edge of the TRIGGER pulse, generated by PCD image sensor, provided an excellent reference signal for the sample and hold device. The generated TRIGGER pulse coincides with the most stable portion of the image sensor analog signal (see Figure 2.20). Once sampled, an ADC digitizes the stored analog signal. Based on the system clock frequency of 200 kHz, the analog signal would require sampling every 20 μsec. The sample-and-hold device would be required to sample and save the signal in the 5 μsec corresponding to the time that the TRIGGER is pulsed on. An independent AD converter would be allocated 15 μsec to complete the acquisition process and perform the digital quantization of the analog data. The quantization accuracy of AD converter is constrained by the PCM encoder which processes a maximum of 10-bits/word.

The third alternative called for the direct AD conversion of the analog signal. The analog signal must still be sampled every 20 μsec; however, the sample-and-hold device would not be used in this implementation. The ADC would be required to digitize the analog signal during the 5 μsec period that the TRIGGER is pulsed on. This implementation demonstrates the tradeoff between utilizing a simple circuit (sample and hold device removed) and a more costly circuit (faster AD converter).

2. Data Storage

The PCM encoder data transmission requirements (Figure 2.5) mandate that the 512 pixels of analog data generated by the PCD image sensor in one integration period be processed and transmitted every 51.2 msec. Furthermore, the PCD image sensor operational requirements (Figure 2.20) demonstrate that only 10.24 msec is required to process the 512 pixels of acquired data generated each integration period. The storage device must be capable of storing the generated data independent of the PCM encoder data access requirements due to the asynchronous nature of the acquisition and transmission operations.

Two methods of data storage were considered. Random access memory (RAM) was considered as a space-efficient alternative allowing for easy access to a large quantities of data. Secondly, a first-in/first-out (FIFO) memory device was considered as an operationally efficient alternative allowing for simple clock control of the read and write cycles. Each device can be configured to perform the same asynchronous read and write functions. The use of RAM requires the implementation of an input and an output counter to indicate the current write and read memory locations. Clocks may be used to advance the memory counters as required. The FIFO can utilize clocked inputs directly to asynchronously read and write the data. One concern with utilizing FIFOs is that, as a general rule, they do not have the data storage capacity

found in RAM. The storage device must have the capacity to assimilate the data accumulation as it occurs during the first 10.24 msec of each communication frame (see Figure 2.5). The data accumulation occurs as a result of the differing read and write data rates. The maximum required data storage is 384 words (10-bits/word).

3. Data Access by PCM Encoder

The PCM encoder will access the data as outlined in Figure 2.5. To access all of the data acquired and stored in one integration period requires 51.2 msec. The interface electronics must "setup" the stored data ensuring the data is available when the PCM encoder accesses the respective digital data line. (Figure 3.2 illustrates the "READ" reference signals provided by the PCM encoder.) The PCM encoder requires a signal level of 3.0 v or greater (maximum 35 v) to guarantee a logic "1" and a signal level of 2.0 v or less (minimum -35 v) to guarantee a logic "0". An open circuit input will be recognized as a logic zero. Once the data is made available, it must remain stable for the one half word period prior to the next word pulse (25 μsec). The requirement for stable data suggests that a digital latch would provide an appropriate interface between the memory device and the PCM encoder.

4. Power Sources

To complement the modular design concept, all of the power required to support MUSTANG operation should be provided

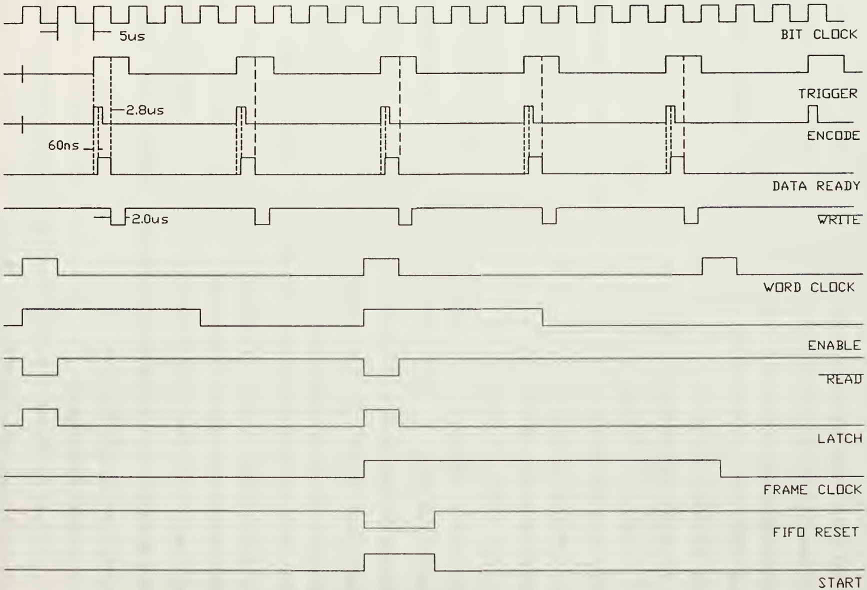


Figure 3.2 Required System Control Signals

via the interface circuitry. MUSTANG requires $\pm$ 15 v to support analog circuit operation, a 0-10 v reference signal for the HV power supply, and 5 v to support digital circuit operation and the HV power supply (Figure 2.21). The 5 and dual 15 v power supplies are modular components installed in the electronics section of the rocket.

Recent rocket experiments have verified that arcing occurs when HV power supplies are operated in a partial vacuum. The phenomenon of arcing is most probable as the rocket transitions from the earth's environment into the experimental environment (altitude of about 100 km). Gasses in the vicinity of the arc tend to ionize establishing inconsistencies in the gasses and their constituents. These inconsistencies will adversely impact the accuracy of the data collected during the experiment. To reduce the risk of arcing and subsequent experimental data degradation, NASA has provided a redundant multi-function timer (WFF 30 Channel Multi-function Timer) to control in-flight events. The sequence of events is as follows:

- Program ON	1.0 sec
- Relay Reset ON	10.0 sec
- Relay Reset OFF	50.0 sec
- HIRAAS Experiment ON MUSTANG Experiment ON	60.0 sec
- Door Open ON	66.0 sec
- Door Open OFF	90.0 sec

- HIRAAS HV ON 110.0 sec
  MUSTANG HV ON

- HIRAAS HV OFF 513.0 sec

- Door Close ON 517.0 sec

- HIRAAS Experiment OFF 523.0 sec
  MUSTANG HV and Experiment OFF

- Program OFF 555.0 sec.

The event sequence timers provide control signals to relays (Deutsch, see Appendix F for details) which, in turn, control the power distribution. Chapter IV will discuss the operation of the relay box in detail. [Ref. 8]

The 0-10 v reference voltage must be generated by the interface board as no other source of variable voltage exists. The reference voltage controls the Microchannel Plate input voltage and ultimately the amplification characteristics of the image intensifier [Ref. 7]. Calculations by the NPS Physics department have concluded that the reference voltage should be adjusted to 10 v [Ref. 9].

B. FINALIZED CIRCUIT DESIGN

Figure 3.3 presents the design that functionally interfaces the MUSTANG detector with the system telemetry. The design can be segregated into four distinct functional structures: data acquisition, data storage, data transmission, and reference signal generation. Figures 2.6 and 2.20 illustrate the reference signals generated by the PCM encoder and the MUSTANG detector respectively. Utilizing

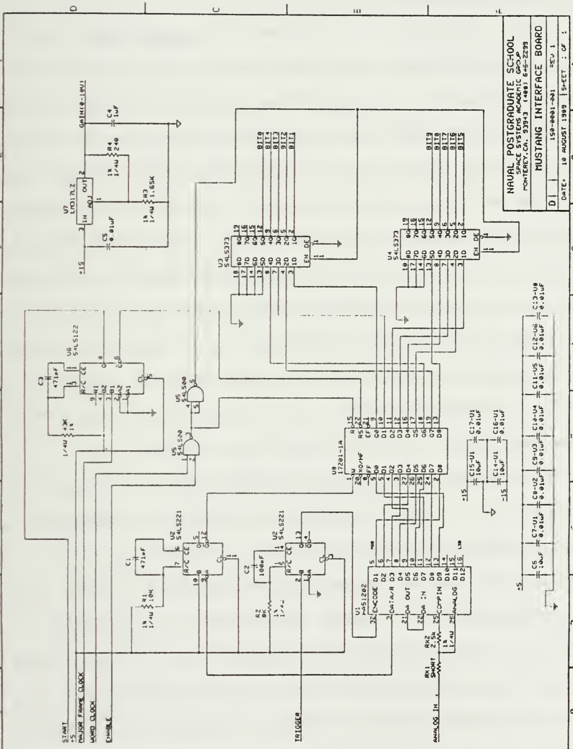


Figure 3.3 System Schematic

selected reference signals (Figure 3.2) with the interface design provides an operationally complete instrument.

1. Data Acquisition

Data acquisition is initiated by the FRAME clock (Figure 3.2). The FRAME clock pulse length is one word period in duration (50 μsec). The 54LS122 monostable triggers on the rising edge of the FRAME clock and generates a 10 μsec START pulse. To insure initialization of the PCD image sensor, the START pulse must be at least 500 nsec in duration. A 10 μsec START pulse is required to meet the reset limitations imposed by the memory device (explained in the next section). The PCD image sensor generates a TRIGGER signal which is synchronized by the leading edge of the START pulse. The TRIGGER signal is on for one BIT period (5 μsec) and off for three BIT periods. The TRIGGER signal is synchronized to correspond with the most stable region of the analog signal.

The leading edge of the TRIGGER signal triggers the first monostable on the 54LS221. The monostable generates a 550 nsec ENCODE pulse (a minimum of 150 nsec is required) which is used to initialize and trigger the HAS1202 ADC. The HAS1202 will perform a 12-bit conversion in a maximum of 2.8 μsec. Although the ADC has a resolution of 12 bits, the PCM encoder will process only 10 bits of data per word. The nine most significant bits generated by the ADC will be stored in memory (the memory can store only 9 bits), the three

remaining least significant bits will be ignored. The 12-bit AD converter was selected based on cost and availability of the component.

2. <u>Data Storage</u>

The leading edge of the ENCODE pulse triggers the DATA READY signal. The DATA READY signal will go high 60 nsec after the ENCODE pulse leading edge. The DATA READY signal will remain high until the AD conversion is complete (a maximum of 2.8 μsec). The falling edge of the DATA READY signal will trigger the second monostable on the 54LS221 to generate a 2 μsec WRITE signal. The CMOS 512 by 9 bit FIFO (IDT7201SA) was selected for the project. Selection, once again, was based on availability and cost of the device. The WRITE signal triggers the FIFO which, in turn, reads the nine most significant bits of data from AD converter. The data will "fall through" the FIFO and will be stored in the subsequent unfilled memory location. The WRITE function is independent of any ongoing READ functions.

As mentioned above, the required waveshape of the start pulse is dictated by the reset requirements of the FIFO (see Appendix I for details). Figure 3.2 illustrates that the RESET signal is the inverse of the START signal. Prior to the RESET signal going high, the FIFO requires the WRITE and READ signals to be high for 120 nsec. The RESET signal must go low for a minimum of 120 nsec to guarantee proper reinitialization. Once the RESET returns high, the READ and WRITE

signals must remain high for a minimum 20 nsec. To ensure all the timing requirements associated with the resetting of the FIFO are met, the RESET signal will remain low for 10 μsec.

3. Data Transmission

Data is read from memory as requested by the PCM encoder. The READ signal is generated when the WORD clock and the ENABLE pulse are "nanded" together. The inverse of the READ signal is the LATCH signal which allows 9 bits of digital data to be loaded into the output latch (2-SNJ54HC373). The PCM encoder allows a data setup time of 25 μsec referenced to the leading edge of the current WORD period. While the data is being read, it must remain stable for the remaining 25 μsec of the current WORD period. The current circuit configuration will transfer data to the output latch in 5 μsec and allow the data to remain latched and stable for 45 μsec. CMOS latches are used to ensure that the "logic 1" was 3 v or greater as required by the PCM encoder.

4. Reference Signal Generation

A 10.0 v reference signal used to support the HV power supply operation was generated utilizing a three-terminal adjustable regulator (LM317LZ). The regulator input is 15 vdc and the input signal is provided via the HV control relay. During the experiment, both the 5 v supply power and the 10.0 v reference signal will be applied simultaneously to the HV power supply as described in the mission sequence of events described above.

C. POWER SUPPLY CALCULATIONS

Prior to flight, the power consumption must be determined to ensure proper selection of flight batteries. During the design phase, power consumption was based on the worst-case (highest power consumption) values provided by the respective component databooks. This estimation was refined and verified by measurement once the flight instrument became operational. Direct measurements by a voltmeter across the power supply output and an in-line ammeter established that 410 ma at 5 v and 130 ma at 15 v will be required to support instrument operation. Battery consumption was calculated as follows:

$$\text{Battery Consumption} = \text{5 v Supply Power} + \text{15 v Supply Power} \quad (3.1)$$

$$= 5.32 \text{ watts} + 6.44 \text{ watts} \quad (3.2)$$

$$= 11.76 \text{ watts} \quad (3.3)$$

The power required to support the 5 v Supply is calculated from Figure 3.4 and the power required to support the 15 v Supply is calculated from Figure 3.5.

Figure 2.21 illustrated the rocket power distribution. The sequence of events established the need for 460 seconds (approximately eight minutes) of instrumentation power. The anticipated total power requirement (HIRAAS and Mustang) is 1200 ma at 28 v for a period of 460 secs. The combined experiments will utilize 0.16 AH of the available 0.62 AH of battery power.

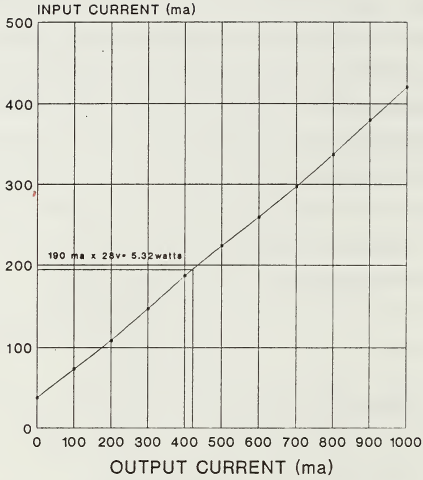


Figure 3.4 Bus Power Required to Support 5 v Power Supply

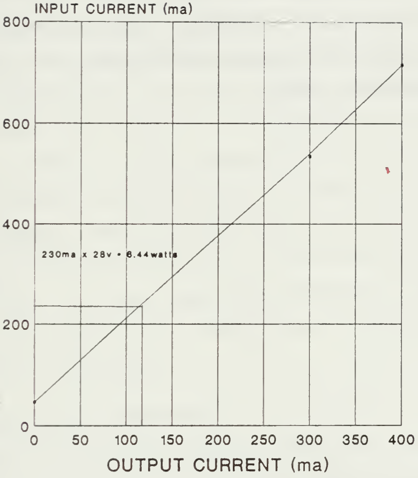


Figure 3.5 System Bus Power Required to Support 15 v Power Supply

Once the interface board became operational, the detector and the interface board were ready for laboratory testing. Further circuit development was required to couple the detector and MUSTANG interface board to a system that simulated the rocket PCM encoder. The simulated encoder and the interface test equipment is referred to as the Ground Support Equipment (GSE).

IV. DESIGN OF GROUND SUPPORT EQUIPMENT

To support the testing and the alignment of the MUSTANG instrument, Ground Support Equipment (GSE) was designed and implemented. The GSE provides instrument support in two operating environments. With GSE support, MUSTANG can be operated in the laboratory where the instrument is tested and aligned. The GSE can also be utilized for in-place preflight testing to ensure the proper operation of both the instrument and the sounding rocket telemetry and control system. The block diagram provided in Figure 4.1 illustrates the possible GSE options. To fully appreciate MUSTANG and the GSE interface, knowledge of the sounding rocket electrical wiring configuration is required.

A. MUSTANG WIRING DESCRIPTION

MUSTANG and HIRAAS are independently operated instruments. The actual interfacing of the two experiments is carried out in the electronics section of the sounding rocket (see Figure 3.1). Common wiring is provided by NASA from the telemetry and control section to the electronics section of the rocket. In the electronics section, the experiments are separated ensuring experimental independence. Experimental independence ensures that a failure of one experiment will not adversely

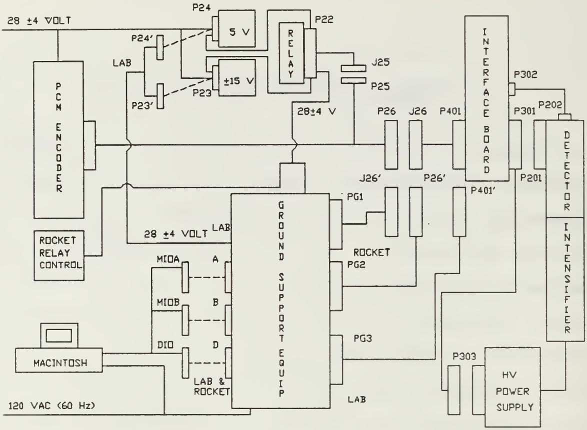


Figure 4.1 Block Diagram of GSE MUSTANG Interface

impact the operation of the remaining experiment. Figure 4.2a illustrates the electrical wiring configuration required to support the in-flight experiment [Ref. 10]. Operation of MUSTANG in a testing configuration will be discussed in the next section.

Five subsystems are mounted in the electronics section to support MUSTANG. These subsystems are illustrated in Figure 4.2b and include:

- Power Supplies (designed by RSI)
- Relay Box [Ref. 11]
- HV Safety Jumpers
- 28 v Distribution Box
- GSE Interface Connectors.

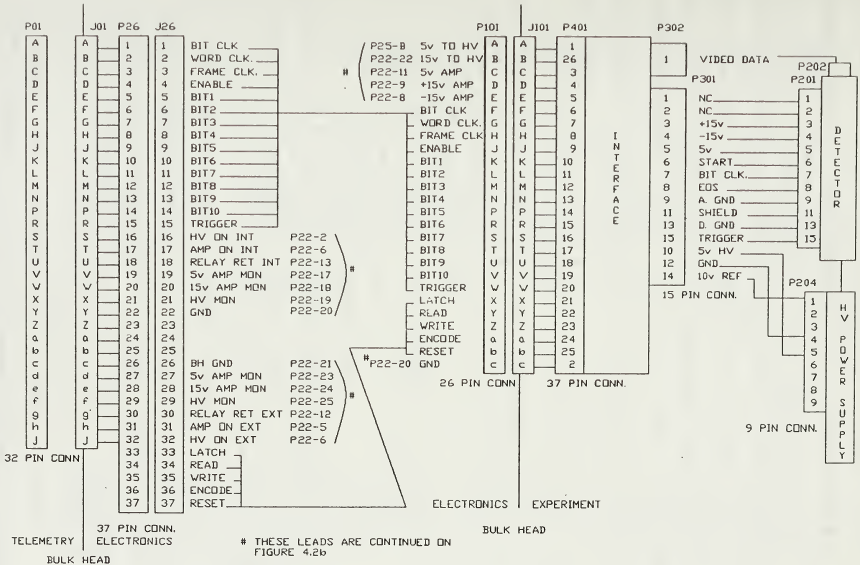


Figure 4.2a Wiring Diagram Required to Support MUSTANG [after Ref. 9]

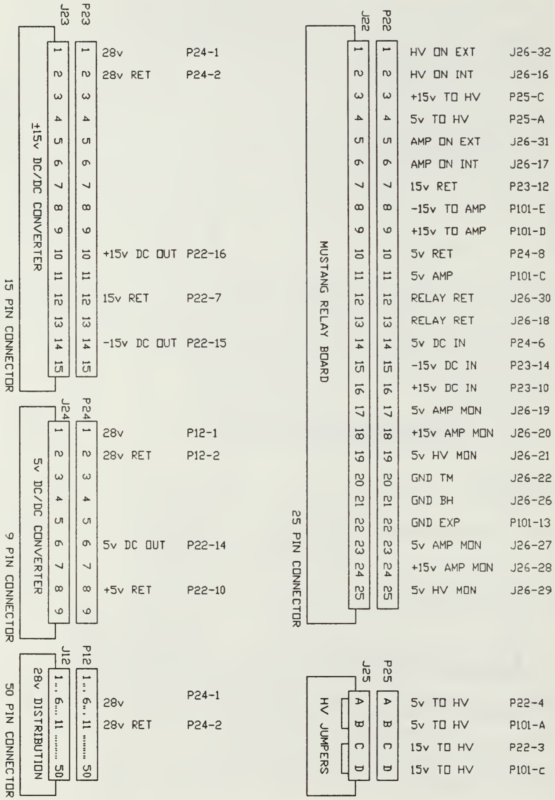


Figure 4.2b Support Components Required to MUSTANG [Ref. 9]

Experimental power is provided by the sounding rocket 28 v unregulated bus. The unregulated power is distributed to both MUSTANG and HIRAAS through the 28 v distribution box. The distribution box is the subsystem where the two experiments are separated. The power supplies (± 15 v and 5 v) convert the unregulated power into the appropriate regulated power to support MUSTANG's analog and digital loads. The power is routed via the relay box to the instrumentation (for details see Figure 4.2c).

The relay box is controlled by the flight sequence timers ensuring strict control of the instrument operation. The relay box also splits the regulated power to achieve:

- 5 v instrumentation power
- 5 v support of the HV power supply
- ±15 v instrumentation power
- 15 v support of the HV power supply.

The HV power supply must be carefully controlled to prevent inadvertent energization while testing is in progress. Previous experience by NRL researchers has verified that the HV power supplies operate properly under total vacuum and at Standard Atmospheric Pressure (STP). If the power supplies are operated under a partial vacuum, arcing is probable, resulting in damage to the power supply and surrounding electronics. Personal safety is also a concern when considering the operation of HV power supplies. The subsystems inside the rocket are closely situated and extreme

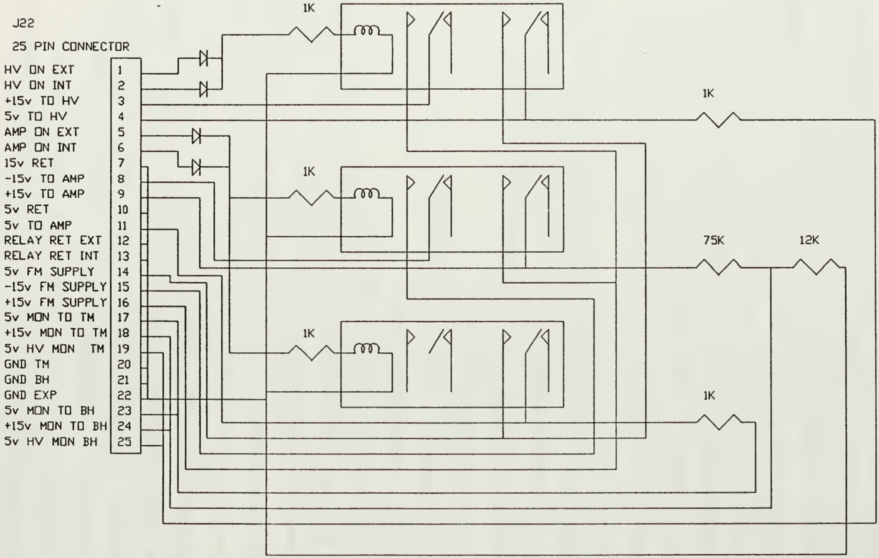


Figure 4.2c MUSTANG Relay Box Schematic [Ref. 10]

care must be exercised to ensure that personnel do not come in contact with energized components powered by a HV power supply. To aid in the control of the HV power supply, jumpers (connector 25) have been installed to interrupt the HV power supply energy source. Finally, the relay box generates monitoring signals which are transferred to the PCM encoder (Chapter II). These monitoring signals are incorporated into the transmitted data stream and provide information on the operational status of the various MUSTANG power supplies.

The GSE connector (connector 26) provides the required interface to externally monitor data when MUSTANG is mounted in the flight configuration. The connector also provides the option of externally controlling MUSTANG when the PCM encoder is unavailable to support flight configuration testing.

B. GSE GENERAL REQUIREMENTS

The GSE is required to support MUSTANG in a variety of operational configurations. In the laboratory, the PCM encoder control signals (see Figure 3.2) are simulated. Laboratory testing is required for MUSTANG initial operational testing and alignment. During rocket integration, operational testing is required to analyze the performance of MUSTANG in the flight configuration. The GSE allows for data accumulation and evaluation in either configuration. The GSE schematic is illustrated in Figure 4.3.

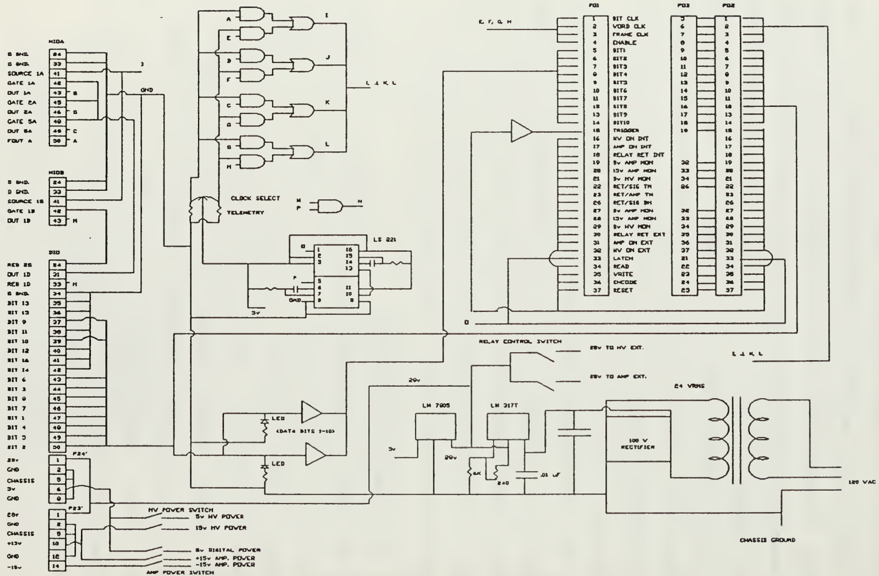


Figure 4.3 Ground Support Equipment Schematic

1. GSE Functions

The GSE schematic illustrates eight basic functions that the system can perform. These eight functions are listed below:

- 28 v power supply to support operation of the 5 v and ±15 v power supplies
- 5 v internal PS to support GSE logic circuits
- Macintosh II computer interface
- ON/OFF control of the 5 v and ±15 v power supplies in both the laboratory and flight configurations
- Clock select circuitry
- Flight configuration test interface
- Laboratory configuration test interface
- Visual data display.

The functions listed above will be described in detail in the following two sections. These functions will be described in terms of their functionality with respect to the appropriate testing configuration.

2. GSE Configuration To Support Laboratory Testing (refer to Figure 4.4)

The Laboratory test configuration is required to support interface circuit testing, MUSTANG alignment, and power supply testing. The PCM encoder is not available in the laboratory environment; therefore all laboratory testing requires the GSE to simulate the PCM encoder. The PCM encoder control signals are generated by the Macintosh II computer

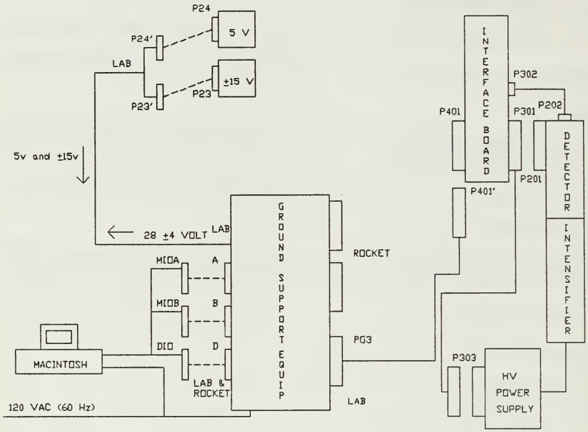


Figure 4.4 Block Diagram Showing GSE in Laboratory Test Configuration

running Labview software (purchased from National Instruments). Three interface boards, designed in two configurations, are installed in the computer. The installed configurations consist of:

- two Multi-function Input/Output (MIO) boards (NB-MIO-16)
- one Digital Input/Output (DIO) board (NB-DIO-32F).

The computer not only generates control signals, but digital data acquisition is also possible with the bit clock running at a frequency of 100 kHz or less. The MIO boards generate

the simulated PCM encoder control signals and the data request signals required by the DIO board. The DIO board is programmed to acquire and plot 512 frames of 10-bit digital data. Each frame of digital data corresponds to one element of the 512-element PCD image sensor. For laboratory operation, the clock select switch should be selected to the computer position.

The GSE generates 28 vdc power at 1.5 A to support testing of the mission power supplies. In the laboratory test configuration, the power supplies are removed from the rocket and are attached to the GSE via the 23' and 24' connectors. In this configuration the relay box is not available to control the sequencing of the power. Two switches (Laboratory Power Sequencing) control both the HV power distribution and the instrumentation power distribution. In the event the flight-configured power supplies are not available, any power supply capable of delivering the rated power may be interfaced using the appropriate connectors at positions P23' and P24'. The 28 v power supply also provides power to a 5 v GSE internal power supply. The internal power supply provides power for the GSE logic circuits and visual data display (10 Light Emitting Diodes-LEDs).

In the laboratory configuration, the GSE is interfaced to MUSTANG utilizing the PG3-P401' jumper. In this test configuration, the PCM encoder and the relay box have been

excluded. The computer will provide the control signals and capture the digital data.

3. GSE To Support Pre-Flight Testing (see Figure 4.5)

Once MUSTANG has been integrated to the sounding rocket, testing is performed to ensure proper operation of the complete flight package. In this configuration the flight-qualified power supplies are installed in the electronics section as illustrated in Figure 4.2b. The HV power supply jumpers (connector 25) may or may not be installed based on the current status of installation and testing. Power

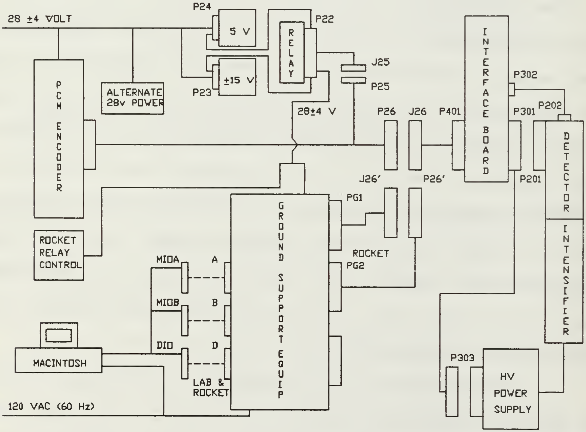


Figure 4.5 Block Diagram Showing GSE in Pre-Flight Test Configuration

sequencing of the system will be controlled by the system timing relays. The PG3-P401' connector is not used and the GSE is interfaced to the sounding rocket via the GSE Interface Connector (connector 26). The computer will not generate control signals in this configuration, but the computer will be available to collect data. The PCM encoder is required to operate as it would in flight. Data transmitted by the rocket may be compared to data accumulated by the computer and system operation can be verified.

An alternate configuration is possible if the telemetry and control electronics are not available for testing. NRL has developed a 28 v power supply that can be externally jumpered to the 28 v Monitor Board (see Figure 4.2b). The jumper at PG1 is disconnected isolating the PCM encoder. The GSE generates a 28 v signal which can be externally applied (see Figure 4.2c) to the relay box. In this configuration, the system control signals will be generated by the computer. Subsequent data collection will also be performed by the computer.

C. GENERAL TESTING

Three basic test configurations have been presented. Detailed analysis of Figure 4.1 suggests that a wide variety of testing configurations are possible. The instrument can be configured to support most any test configuration that the current situation dictates; however, care must be taken to understand the implications of an alternate test setup.

V. CIRCUIT DEVELOPMENT AND TESTING

A. PROTOTYPE DEVELOPMENT AND TESTING

Prototype development was initiated by determining the operating characteristics of the PCM encoder and the PCD image sensor. Discussions with NRL, RSI, and NASA further defined the operating requirements of the MUSTANG interface circuit as discussed in Chapter III. Once the initial background was completed and the desired operating characteristics were defined, the original schematic for the system was designed.

The original system schematic was analytically tested to verify the proper interfacing of MUSTANG and the PCM encoder. The availability of electrical components, specifically the ADC and the FIFO, required changes to be made to the original schematic. Once the changes were implemented, circuit operation was re-verified analytically. Successful completion of analytical circuit verification led to the purchase of the required electrical components (illustrated in Figure 3.3).

The initial operational circuit was layed out on a breadboard and tested for proper operation. At this point in development, the GSE was not available and initial testing was performed using the test circuit illustrated in Figure 5.1. A spare PCD image sensor was purchased and was mounted in a monochromator to support circuit testing. The PCD image

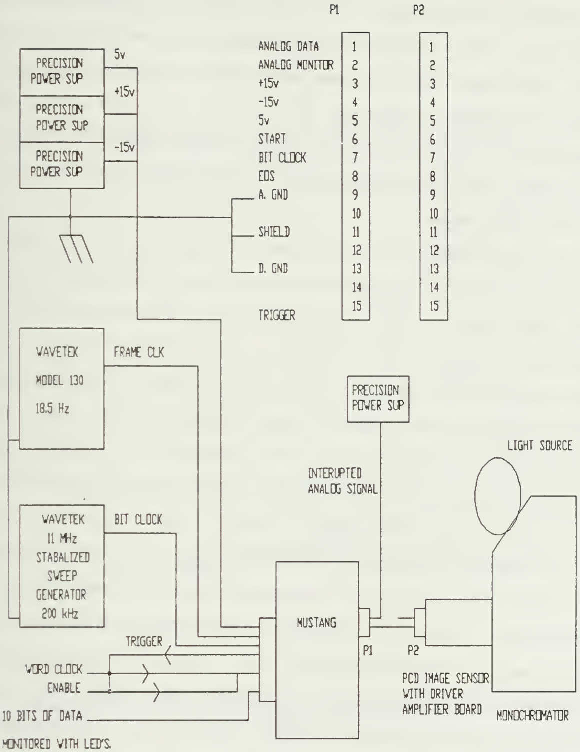


Figure 5.1 Prototype Interface Circuit Test Configuration

sensor, utilized independently of the image intensifier, is a visible light detector. The BIT clock was generated with a Wavetek 11 MHz stabilized sweep generator operating at 200 kHz. The FRAME clock was generated with a Wavetek model 130 function generator operating at 18.5 Hz. The WORD clock was simulated by tieing the TRIGGER pulse to the WORD clock input. The ENABLE pulse was disregarded and the WORD clock was also tied to this input.

Initial testing was performed to determine the linear response of the AD conversion process and to assure proper FIFO operation. Light Emitting Diodes (LEDs) were used to determine digital data output. The detector output was disconnected from the ADC input and a known dc input was applied to the ADC input. The results of the test are illustrated in Figure 5.2a. The response of the ADC was linear but additive noise adversely impacted the AD conversion of analog data (see Figure 5.2b). The observed noise coincided with the edges of the BIT clock and it was apparent that the BIT clock was radiating into adjacent circuit components. The noise component, superimposed on the signal, was a damped sinusoid (ringing) with a frequency of 10 MHz and a maximum zero to peak level of 100 mv. The noise would damp to zero in approximately 0.5 μsec. The initial circuit design did not provide noise reduction capacitors between the power and ground leads of each circuit component as suggested by reputable authors [Ref. 11].

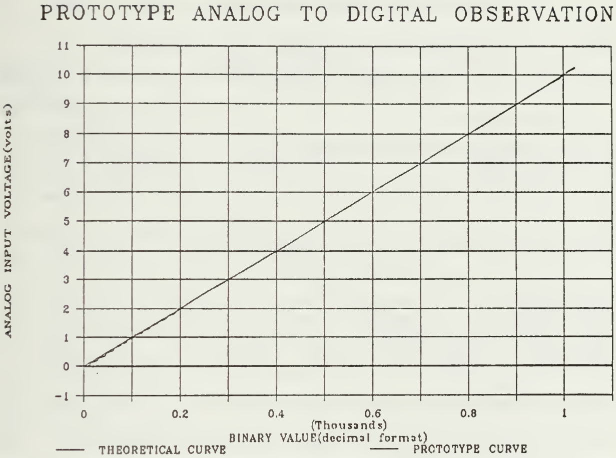


Figure 5.2a Linearity Test for Prototype Interface Circuit

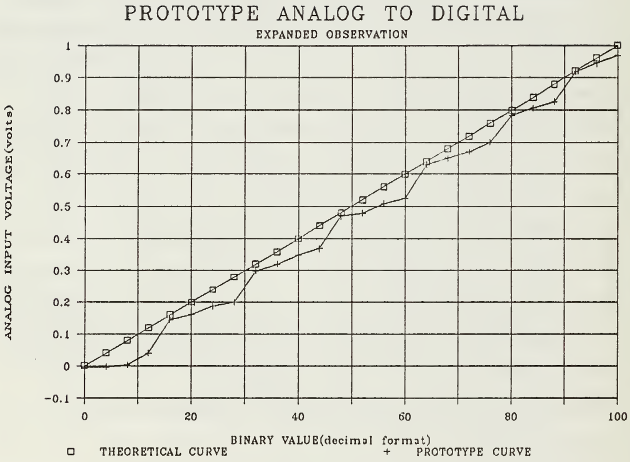


Figure 5.2b Expanded View of Linearity Test for Prototype Interface Circuit

The testing of the bread board circuit validated the MUSTANG interface design. Improved noise reduction was anticipated by implementing a circuit board design and utilizing noise reduction techniques.

B. INITIAL CIRCUIT BOARD DEVELOPMENT AND TESTING

The initial circuit board was designed with noise reduction in mind. The following noise reduction techniques were used:

- The high frequency noise, superimposed on the power leads, was suppressed by establishing a high frequency ground path using a parallel combination of 0.01 μF and 10.0 μF capacitors.
- Analog ground leads were separated from digital ground leads and the ground leads were tied together as far as possible from the interface circuitry.
- Each circuit component power lead was filtered by placing a 0.01 μF capacitor between the power and ground pins. This capacitor was placed as close as possible to the component to minimize lead length and subsequent interference from adjacent leads.

The board was fabricated utilizing a milling machine designed for cutting circuit boards. The testing configuration of Figure 5.1 was utilized to validate the circuit design. The testing results are documented in Figure 5.3. Comparison of Figures 5.2 and 5.3 confirm the improved noise performance of the initial circuit board over the prototype circuit (discussed above in part A). The influence of noise, on the prototype circuit, resulted in nonlinear performance of the three least significant bits (80 mv, 40 mv, 20 mv bits). When the initial circuit board was tested, only the least

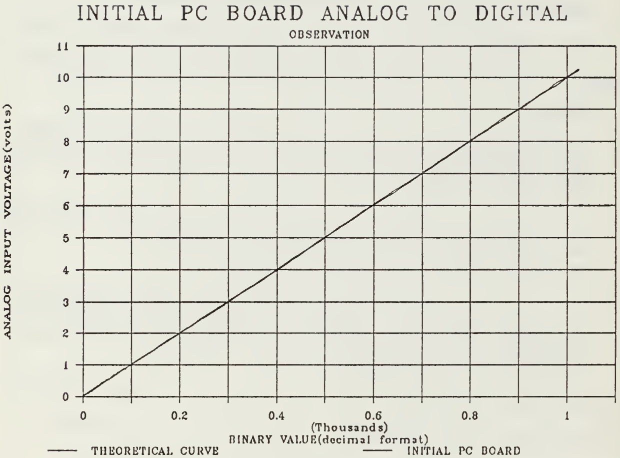


Figure 5.3a Linearity Test for Milled Interface Circuit

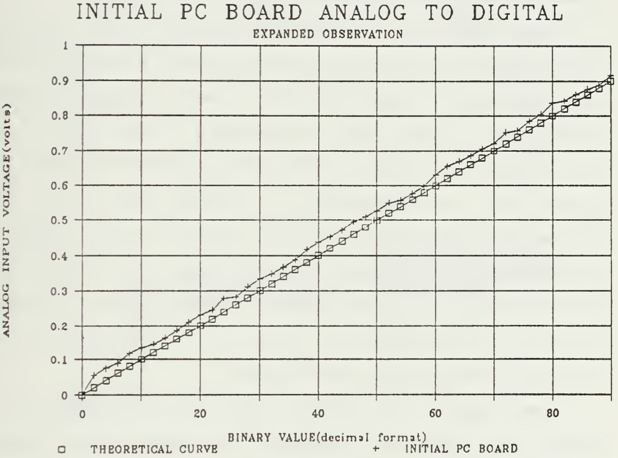


Figure 5.3b Expanded View of Linearity Test for Milled Interface Circuit

significant bit (20 mv bit) had a nonlinear response. Oscilloscope measurements of the analog data signal revealed that the peak to peak amplitude of the superimposed noise had been reduced from 100 mv to 12 mv. The initial circuit board reduced the noise by a factor of eight while maintaining a linear AD conversion characteristic. [Ref. 11]

Close examination of the AD conversion timing sequence verified that the conversion of the two least significant bits was occurring 2.5 μsec after the leading edge of TRIGGER pulse. The 2.5 μsec delay corresponded to both the falling edge of the BIT clock and the maximum observed noise (see Figure 5.4). Readjustment of the ENCODE pulse width (see Figure 3.3) resulted in the AD conversion being completed prior to the falling edge of the BIT clock. By advancing the AD conversion, the adverse impact of noise on the digitizing process was eliminated (see Figure 5.5). Validation of the interface circuitry was now complete.

Upon completion of circuit validation, development of a formal test circuit was initiated. The test circuit, known as the GSE (see Chapter IV), was developed to support a variety of testing requirements. The GSE design was validated by operationally testing a prototype constructed on a breadboard. During this test, the Macintosh computer generated all of the system clocks and collected the digitized video data. The development of the GSE resulted in the ability to

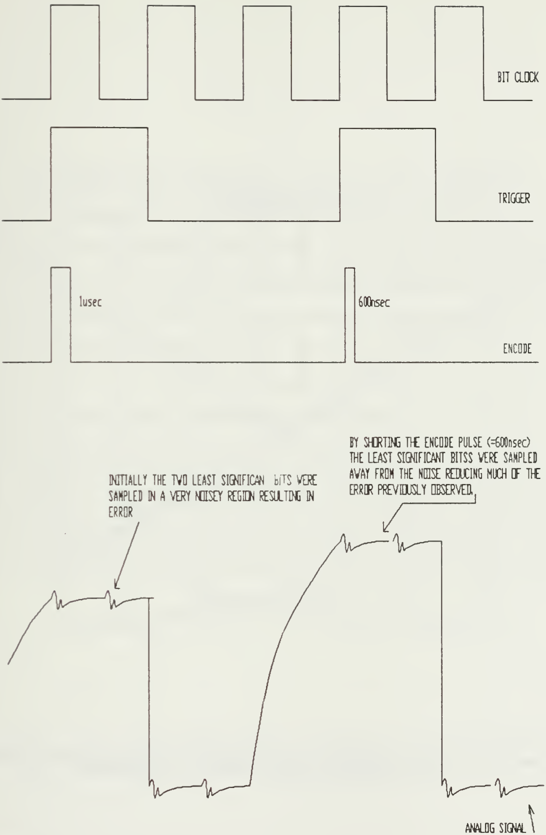


Figure 5.4 Illustration of the Impact of the ENCODE Pulse Width on Digital Data Errors

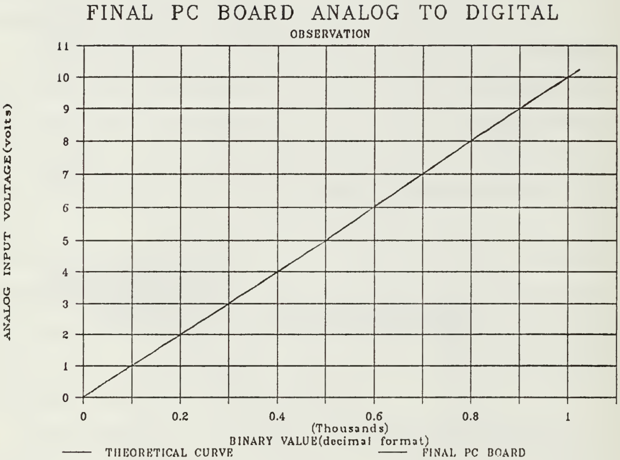


Figure 5.5a Linearity Test for Milled Interface Circuit after ENCODE Pulse Width Adjustment

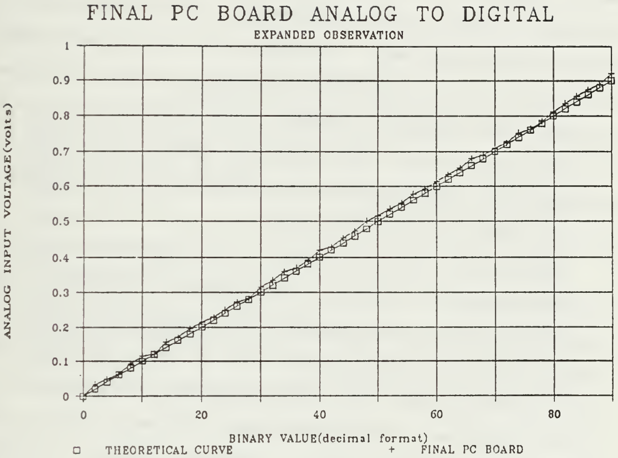


Figure 5.5b Expanded View of Linearity Test for Milled Interface Circuit after ENCODE Pulse Width Adjustment

acquire an accurate visible mercury spectrum. Figure 5.6 illustrates three spectrums which were obtained using a mercury light source and the monochromator. The observed mercury spectrum consisted of one green line at 5461 Å and two yellow lines at 5770 Å and 5791 Å. With the light slit completely closed on the monochromator, the dark response of Figure 5.6a was obtained. From Figure 2.14, the expected dark response at 25° C is 90 mv. The theoretical response of 90 mv validated the observed response of 80 mv to 100 mv. In Figures 5.6b and 5.6c, the light slit opening was varied to confirm proper operation of the interface circuit and GSE over the full range of light intensity.

During this stage of testing, it was determined that the Macintosh computer, running in the Labview environment, was incapable of accurately acquiring data when the BIT clock was operated at a frequency greater than 120 kHz. By observing the digitizing process with the oscilloscope, proper operation of the interface circuit and GSE was confirmed with the BIT clock operating at 200 kHz. Follow-on trouble shooting verified that when the BIT clock was operated at a frequency greater than 120 kHz, the computer could not retrieve all the data sent to the interface circuit output buffer. At a BIT clock frequency of 200 kHz, the computer would miss one third of the data. The remainder of the testing was performed at 100 kHz, noting that the observed spectrum amplitudes would be two times greater than the spectrum amplitudes observed at

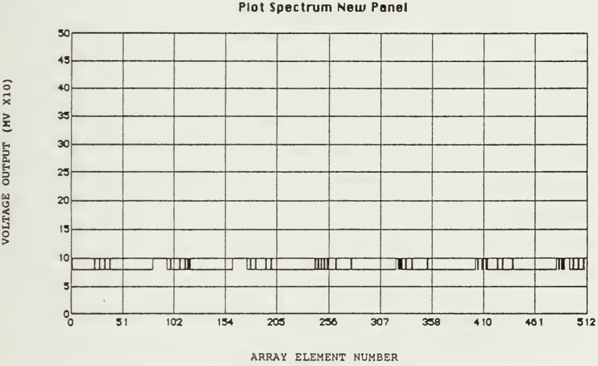


Figure 5.6a Dector Response with no Light Present (Dark Counts)

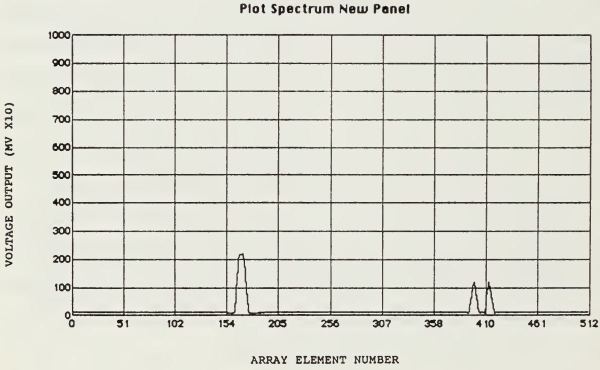


Figure 5.6b Visible Mercury Spectrum with Monochromator Slit Partially Open

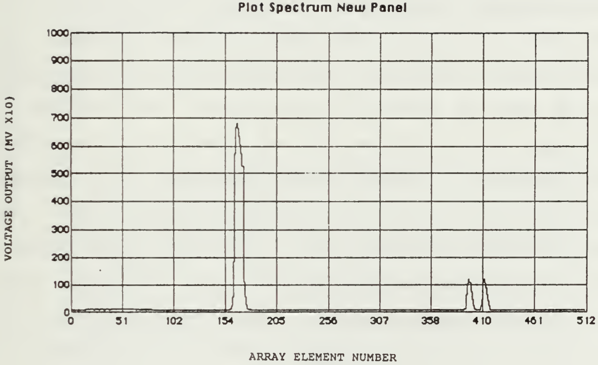


Figure 5.6c Visible Mercury Spectrum with Monochromator Slit Open to the Point of PCD Image Sensor Saturation

200 kHz. The two-fold increase in spectrum amplitude is directly proportional to the increased integration time. Once the GSE testing was completed satisfactorily, the permanent test equipment was fabricated as described in Figure 4.3.

C. FINAL CIRCUIT BOARD FABRICATION, INTEGRATION, AND TESTING

From the schematic used to generate the initial milled interface circuit board, artwork for an etched circuit board was fabricated. Two etched interface circuit boards were purchased and populated (one board served as a backup). A flight chassis was milled from aluminum, and the interface circuit board was installed in the chassis. NRL provided an instrument mounting bracket that was a replica of the flight mounting bracket. Research Support Instruments (RSI) mounted the flight detector onto the replicated mounting bracket and sent the assembled system to NPS. At NPS, the flight chassis was secured to the mounting bracket. The final cable runs were fabricated and installed. MUSTANG was now completely assembled and ready to undergo the final phase of testing.

The final phase of testing was performed by operating MUSTANG in a known ultraviolet (UV) environment. Testing was performed utilizing the laboratory test configuration described in Chapter IV (see Figure 4.4). A mercury light source was used to illuminate the instrument resulting in the spectrum recorded in Figure 5.7 (single spectral line occurs at a wavelength of 2537 Å). The observed spectrum matched the

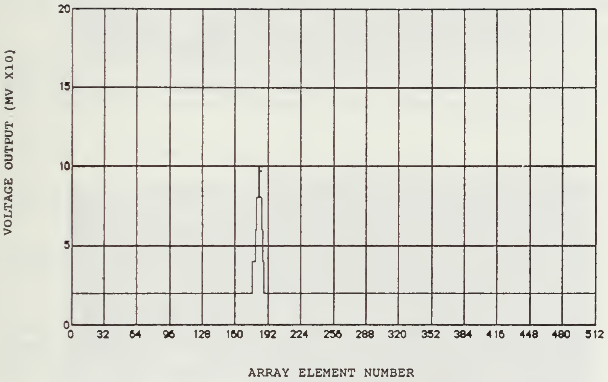


Figure 5.7 Mercury Ultraviolet Spectrum

predicted wavelength response of a mercury spectrum thereby validating the operation of MUSTANG.

D. SYSTEM INTEGRATION AND ILLUSTRATIVE PHOTOGRAPHS

Photographs of the integrated flight instrument system have been provided in Figures 5.8-5.14. Additionally, sample waveforms have been included for general interest. All clocked waveforms were generated by the Macintosh computer operating in the Labview environment. The following is a brief synopsis of each photograph:

- Figure 5.8 illustrates MUSTANG configured in a laboratory test environment. Pictured equipment includes the Macintosh computer, GSE, 5 and $\pm$15 v power supplies, and the detector

- Figure 5.9 illustrates the flight interface circuit (fabricated and assembled at NPS)

- Figure 5.10 illustrates the 10 kHz WORD clock (bottom) referenced to the 100 kHz BIT clock (top)

- Figure 5.11 illustrates the TRIGGER signal (bottom) referenced to the 100 kHz BIT clock (top). There are four BIT clock cycles to each TRIGGER period

- Figure 5.12 illustrates the ENABLE pulse (bottom) referenced to the to the 10 kHz WORD Clock (top). There are 16 WORD pulses for each ENABLE pulse representing the 16 WRITE commands required for each row of the communication frame

- Figure 5.13 illustrates the AD conversion of the least significant bit (bottom) referenced to the TRIGGER signal (top)

- Figure 5.14 illustrates the FRAME period of 102.4 msec. The pulse width is small (600 nsec) in relation to the periodicity of the signal.

Figure 5.8 Detector and Test Equipment in Laboratory Test Configuration

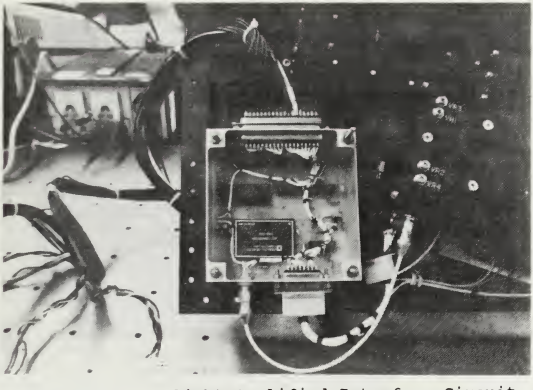


Figure 5.9 Flight Qualified Interface Circuit

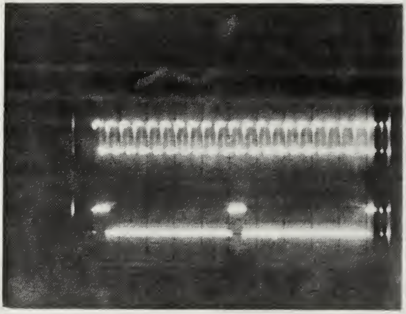


Figure 5.10 Computer-Generated BIT Clock (Top) and WORD Clock (Bottom)
(Vertical Scale: 5 v/div, Horizontal Scale: 20 μsec/div)

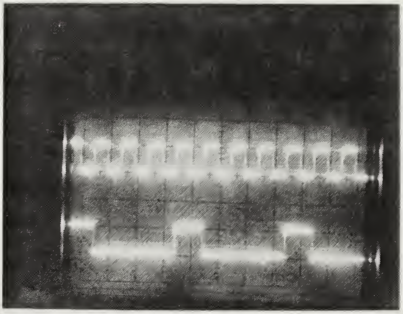


Figure 5.11 Computer-Generated BIT Clock (Top) and TRIGGER (Bottom)
(Vertical Scale: 5 v/div, Horizontal Scale: 10 μsec/div)

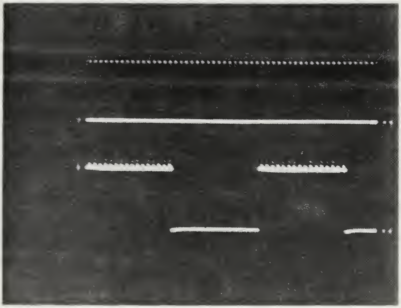


Figure 5.12 Computer-Generated WORD Clock (Top) and ENABLE (Bottom)
(Vertical Scale: 2 v/div, Horizontal Scale: .5 msec/div)

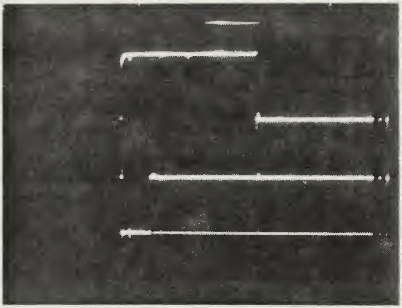


Figure 5.13 TRIGGER Signal (Top) and the Digitizing of the Least Significant Bit (Bottom)
(Vertical Scale: 2 v/div, Horizontal Scale: 2 μsec/div)

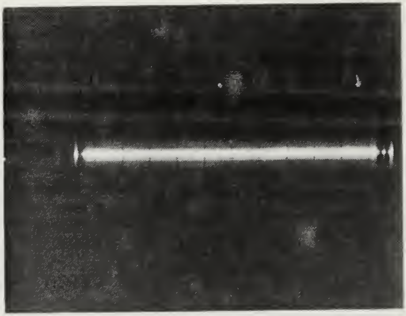


Figure 5.14 FRAME Pulse (Period 102.4 msec)
(Vertical Scale: 2 v/div, Horizontal Scale: 20 msec/div)

By analyzing the photographs, the following conclusions can be drawn:

- The WORD clock is properly synchronized to the BIT clock
- The TRIGGER signal, generated by the PCD image sensor, is properly synchronized to the BIT clock. The TRIGGER pulse width is 1 BIT period
- 16 WORD clock periods occur each time the ENABLE pulse is high. The ENABLE signal has a duty cycle of 50 percent
- The least significant bit is converted by the ADC prior to the falling edge of the BIT clock. The influence of edge noise on the AD conversion of the analog signal is eliminated
- The frame clock period is 102.4 msec.

The photographs documented the proper operation of the MUSTANG interface board and the GSE.

VI. CONCLUSIONS

The development and integration of MUSTANG afforded NPS the opportunity to participate collectively with other organizations in scientific research. The operational theory required for MUSTANG was developed collectively by NPS students and NRL scientists. The Office of Naval Research approved the operational theory and recommended further research. To support continued research, NASA approved a sounding rocket experiment (36.053), scheduled for February 1990. The operational theory evolved into a detector design sponsored by NPS and fabricated by RSI. NPS students actively participated in the integration of the detector to both the rocket platform and the HIRAAS instrument.

During the integration process, electronic circuits were designed, prototyped, tested, fabricated and assembled by NPS students and staff. The MUSTANG interface circuit design evolved as follows:

- The PCM encoder and PCD image sensor operational specifications were studied in detail to determine the interface requirements.
- Operational limitations of the PCM encoder and the PCD image sensor required that the data acquisition and data transmission processes occur asynchronously. A schematic was designed that would support asynchronous operation of the PCD image sensor and the PCM encoder. The schematic consisted of three monostables for waveshaping, one ADC, one memory device, one reference signal generator, and the required wiring to interface the detector to the PCM encoder.

- Using the schematic as justification, the prototype circuit was built and tested. Testing of the prototype validated the asynchronous design criteria; however, the edge noise resulting from the BIT clock was excessive. The excessive noise distorted the data contained in the three least significant bits of the ADC.

- The initial circuit board was engineered and fabricated to validate the artwork for the flight circuit board and to incorporate and test noise reduction techniques. The noise reduction techniques consisted of:

  - providing a high frequency ground for the power leads.

  - providing a high frequency ground for individual component power leads.

  - separating the analog and digital ground leads.

  By using these noise reduction techniques, the noise was reduced by a factor of eight over the prototype circuit. The final noise reduction technique involved the adjustment of the ENCODE pulse width. The pulse width was shortened to 600 nsec ensuring the completion of the AD conversion prior to the falling edge of the BIT clock.

- Based on the artwork produced and validated during the development of the initial circuit board, two flight boards were fabricated.

- To support testing of the flight boards in a variety of operating environments including pre-flight testing, the GSE was designed and built. Integrated testing of the instrument in the laboratory environment validated the proper operation of the interface board and the GSE; however, the data acquisition routine did not function accurately when the BIT clock was operating at 200 kHz. The acquisition routine did operate accurately at 100 kHz; consequently, the remainder of the testing was performed with the BIT clock operating at 100 kHz.

The development and integration of MUSTANG afforded the NPS students the opportunity to actively participate in research beyond the scope of study that is achievable in a classroom environment. Specifically, the MUSTANG experiment

provided the engineering student the opportunity to participate in a program environment. Engineering issues of concern included parts availability, production deadlines, component compatibility, noise reduction, and subsystem integration.

The opportunity for future engineering work related to MUSTANG is uncertain. If the rocket experiment validates the proposed theory, future experiments involving space-based systems are likely. If the proposed theory is not validated by MUSTANG, future research may be devoted to re-engineering the instrument or re-developing the theory.

APPENDIX A

INSTRUMENTATION SYSTEM DESIGN REVIEW PACKAGE

This appendix provides specific technical information pertaining to the following:

- Transmitter
- PCM Encoder Operational Configuration
- RF Link Analysis
- Detailed PCM Encoder Communication Matrix
- PCM Encoder Addressing List
- Comprehensive List of Flight Instrumentation.

June 5, 1989

MEMORANDUM

TO: Paul Buchanan, Payload Manager

FROM: Warren R. Oufrene, Jr., Instrumentation Engineer

SUBJECT: Instrumentation System Design Review Package for Payload 36.053
McCoy/Naval Research Lab

CSC

Introduction

This flight is planned to fly from WSMR in February 1990. The instrumentation design is similar to 36.010 which flew from WSMR in February of 1986. An S-19 guidance system has been added for this flight. The PCM format has been changed to accomodate the added data channels of the S-19 and new experiment. The PCM system will run at 200 Kbit. Also, an electronic timer will be flown this flight.

Telemetry System Description

The TM system contains a 200 Kbit PCM/FM RF link @ 2269.5 MHz. The PCM system is a Vector MMP-600 series Micro-PCM encoder using BIØ-L code. This link contains all experiment data, S-19 data, ACS data, and TM housekeeping data. The transmitter is a 5-watt Vector T105S.

RF carrier deviation, IF and video bandwidth, and safety factor are as follows:

PCM/FM Link (200 Kbit BIØ-L)

Carrier Frequency	2269.5	
Carrier Deviation	$\pm$200 KHz	S_f = 13.7 dB
Receiver 2nd IF Bandwidth	1.0 MHz	
Receiver Video Bandwidth	400 KHz	

A Vega C-Band radar transponder will be used for trajectory data. Associated with this transponder is a 2-way power divider, two phase matched RF cables, and two C-Band antennas mounted physically 180° apart.

Thrust acceleration data is obtained from two accelerometers mounted in the thrust axis. One, a Setra 141A accelerometer is conditioned to a +30G -20G range. The second, an Edcliff accelerometer, has a +17G -1G range and meets the WSMR IIP Program requirements. A $\pm$5G Setra accelerometer will be used in the X-Axis for lateral acceleration data.

Housekeeping data consists of the usual bus voltage monitors, pyro squib current monitors, bus current monitors, and temperature monitors. Recovery system, vehicle and ignition systems are also included in housekeeping data.

Building F-10/WFF
Wallops Island, Virginia 23337
804 824.1298

Please note the following attachments:

1. RF Link Analysis
2. PCM Measurement List
3. PCM Format
4. PCM Stack Arrangement
5. PCM Stack Module Addressing
6. MMP-600 Micro PCM E-Prom Program
7. Instrumentation Components List

Warren R. Dufrene Jr.

Warren R. Dufrene, Jr.

36.053
McCoy/Naval Research Lab
System Parameters

Carrier Frequency	2269.5 MHz
Modulation Type	PCM/FM
Radiated Power	$\geq$5 Watts
Downlink Carrier Deviation	$\pm$200 KHz
Ground Station Receiver	
IF Bandwidth	1 MHz
Video Bandwidth	400 KHz
PCM Code:	BIØ-L
Bit Rate:	200 Kbit/Second
Words/Minor Frame	32
Minor Frames/Major Frame	32
Bits/Word	10
Sync Word #1	1110110111 MSB LSB
Sync Word #2	1000100000
Bit Alignment	MSB First
SFID Counter Location	Word 1
SFID Word	$0002^4 2^3 2^2 2^1 2^0 00$ LSB
# of Bits in ID Counter	5
ID Counter Counts	Up & MSB First
Parity:	None

S_f = Safety Factor (dB's)

S_f = $P_t + D_i + G_t + G_r - S/N - B_f - P_L$

P_t = Transmitter Power = Watts (min.) in dBw = 5 Watts (Min) = 7 dbw

D_i = Diplexer Insertion Loss = -1.3 dB (Not Used)

G_t = Transmitting Antenna Gain = -6 dB WFF Microstrip 17.25" Dia.

G_r = Receiving Antenna Gain = [37.2 dB (Illum. Factor 55%) -3 dB -3 dB (Polarization Mismatch)]

= 31.2 dB (Antenna Gain for 10' Dish)

S/N = Signal to noise ratio in dB = 13 dB for PCM/FM

B_f = $10 \, \mathrm{Log}_{10} \, (KT_SB)$

K = Boltzmann's Constant

B = Receiver 2nd IF Filter Bandwidth

K = 1.38×10^{-23} joules/°K

B = 1,000 KHz

T_S = System Noise Temp.

T_A = Antenna Noise Temp.

T_R = Receiving Noise Temp.

δ = Power transmission coefficient for the transmission - line preceding the pre-amp = .9

T_S = $T_A + T_R$

T_A = $(40°)\delta + 290\,(1-\delta)$

T_A = 36°K + 29°K = 65°K

T_R = $T_{PA} + [T_{DC}/g_{PA}] + [T_c/(g_{PA} \times g_{DC})] + [T_r/(g_{PA} \times g_{DC} \times g_c)]$

T_{PA} = Pre-Amp Noise Temp

T_{DC} = Down Converter Noise Temp

T_c = RF Cable Noise Temp

T_r = Receiver Noise Temp

T_S = (220°K @ WSMR)

B_f = $10 \, \mathrm{Log}_{10} \, (KT_sB) = -145.2$ dB

P_L = Path Loss = $20 \, Log_{10} \, [4\pi \, FR)/C]$

= $20 \, Log_{10} \, F^* + 20 \, Log_{10} R^{**} + 20 \, Log_{10} \, (4\pi /C)$

C = Speed of Light in Km/Sec = 2.9979×10^5 Km/Sec

*F = Freq. in Hz = 2,269,500,000

**R = Range in Km = 360 Km (Max Slant Range)

P_L = 150.7 dB

S_f = 7 dB + (-6 dB) + 31.2 dB - 13 dB - (-145.2 dB) - 150.7 dB

S_f = 13.7 dB

8/4/89

36.053
McCoy/Naval Research Lab
PCM Measurement List

Format Label	Data Description	Time Slot WD	FR	INT	Sample Rate SPS
Parallel Digital Data					
	Bit				
P1	1 MSB Prog Event #1	12	1	8	78
	2 2				
	3 3				
	4 4				
	5 5				
	6 6				
	7 7				
	8 8				
	9 9				
	10 LSB Prog Event #10				
	Bit				
P2	1 MSB Prog Event #11	12	3	8	78
	2 12				
	3 13				
	4 14				
	5 15				
	6 16				
	7 17				
	8 18				
	9 19				
	10 LSB Prog Event #20				
	Bit				
P3	1 MSB Prog Event #21	12	5	8	78
	2 22				
	3 23				
	4 24				
	5 25				
	6 26				
	7 27				
	8 28				
	9 29				
	10 LSB Prog Event #30				

Format Label	Data Description	Time Slot WD	FR	INT	Sample Rate SPS
Parallel Digital Data (cont.)					
	Bit				
P4	1 MSB Prog Event #31	12	7	8	78
	2 32				
	3 33				
	4 Prog Event #34				
	5				
	6				
	7				
	8				
	9				
	10 LSB				
P5-1	Exp Data	15	1	1	625
P5-2		16	1	1	625
P5-3		17	1	1	625
P5-4		18	1	1	625
P5-5		19	1	1	625
P5-6		20	1	1	625
P5-7		21	1	1	625
P5-8		22	1	1	625
P5-9		23	1	1	625
P5-10		24	1	1	625
P5-11		25	1	1	625
P5-12		26	1	1	625
P5-13		27	1	1	625
P5-14		28	1	1	625
P5-15		29	1	1	625
P5-16	Exp Data	30	1	1	625
	Bit				
P6	1 MSB Data	12	4	4	156
	2				
	3				
	4				
	5				
	6				
	7				
	8				
	9				
	10 LSB Data				

Format Label	Data Description	Time Slot WD	FR	INT	Sample Rate SPS
S-19 Data					
A1	Gyro Roll	11	1	1	625
A2	Gyro Pitch	7	2	2	312
A3	Gyro Yaw	8	4	4	156
A4	Roll Resolver $U\theta$	5	1	16	39
A5	Roll Resolver $U\psi$	5	2	16	39
A6	Servo Amp, $S\delta y$	5	3	16	39
A7	Servo Amp, $S\delta z$	5	4	16	39
A8	Servo Rtn, $U\delta y$	5	5	16	39
A9	Servo Rtn, $U\delta z$	5	6	16	39
A10	+15V	2	26	32	19
A11	-15V	4	14	16	39
A12	Batt 1 -18V	5	15	16	39
A13	Batt 2 +28V	5	16	16	39
A14	Batt 3 +8V	2	27	32	19
A15	L.O./Timer Zero	4	15	16	39
A16	Start Guidance	5	7	16	39
A17	Canard Decouple	5	8	16	39
A18	Current Monitor	5	9	16	39
A19	Bottle Pressure	5	10	16	39
A20	Regulated Pressure	5	11	16	39
A21	Module Off Cmd	2	28	32	19
A22	Gyro Cage Cmd	2	29	32	19
A23	Gyro Uncage Cmd	2	31	32	19
A24	Gyro Pitch, Full Scale	5	12	16	39
A25	Gyro Yaw, Full Scale	5	13	16	39
ACS Data					
A26	Roll Valves	8	1	4	156
A27	Roll Position	6	4	4	156
A28	Roll Rate	3	2	16	39
A29	Roll Fine	3	3	16	39
A30	Roll Cosine	3	4	16	39
A31	Pitch Valves	8	2	4	156
A32	Pitch Position	3	5	16	39
A33	Pitch Rate	3	6	16	39
A34	Pitch Resolver	3	7	16	39
A35	Yaw Valves	8	3	4	156
A36	Yaw Position	3	8	8	78
A37	Yaw Rate	3	1	8	78
A38	Yaw Fine	3	10	16	39

36.053
McCoy/Naval Research Lab
PCM Measurement List (cont.)

Format Label	Data Description	Time Slot WD	FR	INT	Sample Rate SPS
ACS Data (cont.)					
A39	Yaw Resolver	3	11	16	39
A40	Slave Roll Position	3	12	16	39
A41	System Mode	3	13	16	39
A42	Int Rig	3	14	16	39
A43	±15V Mon	3	15	16	39
A44	±26V Mon	2	32	32	19
A45	Rig Heater (Roll)	4	1	16	39
A46	Rig Heater (Yaw)	4	2	16	39
A47	5V Reg Mon	4	3	16	39
A48	Bottle Pressure	4	8	8	78
A49	Bottle Temp	4	4	16	39
A50	Reg Pressure	4	5	16	39
A51	Yaw Fine Pressure	4	6	16	39
A52	Roll Fine Pressure	4	7	16	39
TM Housekeeping					
A53	ORSA Sys 1 Sig Mon	4	9	16	39
A54	ORSA Sys 2 Sig Mon	4	10	16	39
A55	ORSA H/S Dply Mon	4	11	16	39
A56	ORSA Pressure Mon	6	7	8	78
A57	Ign SCM 1, Ign, Des, Sep	4	12	16	39
A58	Ign SCM 2, Ign, Des, Sep	4	13	16	39
A59	B.B. Motor Chamber Press	6	6	8	78
A60	B.B. Motor Separation	2	1	32	19
A61	Lanyard Switch #1	2	2	32	19
A62	TM +28V Bus Mon	2	3	32	19
A63	TM +5V Mon	2	4	32	19
A64	Door +28V Bus Mon	2	5	32	19
A65	XMTR Temp	2	6	32	19
A66	PCM Stack Temp	2	7	32	19
A67	IIP Z-Accel (+17 -1G)	9	1	1	625
A68	Z-Accel (+20 -5G)	10	1	1	625
A69	X-Accel (±5G)	7	1	2	312
A70	TM Bus Current	6	1	8	78
A71	XPDR Bus Current	6	2	8	78
A72	Exp Batt 1 Bus Current	6	3	8	78
A73	Door Batt Bus Current	6	5	8	78
A74	N/C Breakwire	2	8	32	19
A75	Timer +5V	2	9	32	19
A76	Lanyard Switch #2	2	10	32	19

36.053
McCoy/Naval Research Lab
PCM Measurement List (cont.)

Format Label	Data Description	Time Slot WD	FR	INT	Sample Rate SPS
TM Housekeeping (cont.)					
A77	Exp Hi-Voltage Mon #1	2	11	32	19
A78	Exp Hi-Voltage Mon #2	2	12	32	19
A79	Exp Batt 2 Bus Mon	2	13	32	19
A80	Exp Aspect Relay Mon	2	14	32	39
A81	+15V DC/DC Mon	2	15	32	19
A82	∓5V DC/DC Mon	2	16	32	19
A83	Exp Spare	2	17	32	19
A84	Film Advance Mon	12	2	8	78
A85	Door Position Mon	12	6	8	78
A86	Batt 1 +28V Mon	2	18	32	19
A87	Batt 2 Mon	2	19	32	19
A88	Door Open/Close	2	20	32	19
A89	Sequence Mon	2	21	32	19
A90	+5V Amp Mon	2	22	32	19
A91	+15V Amp Mon	2	23	32	19
A92	+5V HV Mon	2	24	32	19
A93	Skin Temp Mon	2	25	32	19
A94	Timer #1 Data	13	1	1	625
A95	Timer #2 Data	14	1	1	625
A96	ACS Start Mon	5	14	16	39

36.053
McCoy/Naval Research Lab
PCM Stack Module Addressing
(Hardwire)

Component	Address A7	A6	A5	A4	A3	A2	A1	A0		
PD629 #1	0	0	0	0	0	1	X	X		
PD629 #2	0	0	0	0	1	0	X	X		
MP-601L #1	0	0	1	X	X	X	X	X		
MP-601L #2	0	1	0	X	X	X	X	X		
MP-601L #3	0	1	1	X	X	X	X	X		
Sync #1 Inst	1	1	1	0	1	1	0	1	1	1
Sync #2 Inst	1	0	0	0	1	0	0	0	0	0

Pattern Length	Pattern
20	11101101111000100000

36.053
McCoy/Naval Research Lab

TM PCM Format
Bit Rate: 200 Kbit
Code: BIØ-L
625 SPS/Word

Bits/Word: 10
Parity: None
Align: MSB First
Word Rate: 20K Words/Sec

Subframe ID: Word 1
Subframe Sync Pat: 000XXXXX00
Frame Sync Pat: 20 Bits
Frame Sync Words: 31, 32

FS1: 1110110111
FS2: 1000100000

Subframe ↓ Word →

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
1	SFID	A60	A37	A45	A4	A70	A69	A26	A67	A68	A1	P1	A94	A95	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	FS1	FS2
2		A61	A28	A46	A5	A71	A2	A31				A84																				
3		A62	A29	A47	A6	A72		A35				P2																				
4		A63	A30	A49	A7	A27		A3				P6																				
5		A64	A32	A50	A8	A73		A26				P3																				
6		A65	A33	A51	A9	A59		A31				A85																				
7		A66	A34	A52	A16	A56		A35				P4																				
8		A74	A36	A48	A17	A27		A3				P6																				
9		A75	A37	A53	A18	A70		A26				P1																				
10		A76	A38	A54	A19	A71		A31				A84																				
11		A77	A39	A55	A20	A72		A35				P2																				
12		A78	A40	A57	A24	A27		A3				P6																				
13		A79	A41	A58	A25	A73		A26				P3																				
14		A80	A42	A11	A96	A59		A31				A85																				
15		A81	A43	A15	A12	A56		A35				P4																				
16		A82	A36	A48	A13	A27		A3				P6																				
17		A83				A70		A26				P1																				
18		A86				A71		A31				A84																				
19		A87				A72		A35				P2																				
20		A88				A27		A3				P6																				
21		A89				A73		A26				P3																				
22		A90				A59		A31				A85																				
23		A91				A56		A35				P4																				
24		A92				A27		A3				P6																				
25		A93				A70		A26				P1																				
26		A10				A71		A31				A84																				
27		A14				A72		A35				P2																				
28		A21				A27		A3				P6																				
29		A22				A73		A26				P3																				
30		A80				A59	↓	A31				A85																				
31	↓	A23				A56	A69	A35	↓	↓	↓	P4	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
32	SFID	A44	↓	↓	↓	A27	A2	A3	A67	A68	A1	P6	A94	A95	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	P5	FS1	FS2

36.053
McCoy/Naval Research Lab
Instrumentation Components List

Item	Qty	Component	Mfg	Model	Comments
1	1	S-Band Transmitter	Vector	T105S	2251.5 MHz
2	1	Transponder	Vega	302C-2	C-Band
3	2	Transponder Ant	PSL	7.015	Rams-Horn
4	1	Transponder Pwr Div	Vega	853-C2	
5	3	Thermisters	Fenwall	Isocurve	15K Ohm
6	1	Accelerometer	Edcliff	7-101	+17 -1G, Z-Axis
7	1	Accelerometer	Setra	141-A	+20 -5G, Z-Axis
8	1	Accelerometer	Setra	141-A	±5G, X-Axis
9	2	Accelerometer Cond Box	WFF	--	
10	2	Current Mon Boxes	WFF		
11	4	Current Sensors	F.W. Bell	MB-1020	
12	1	Diode Logic Mon Box	WFF		
13	1	Pyro Mon Box	WFF		
14	1	TM Mon Box	WFF		
15	1	S-Band Antenna	Ball Bros	S/N 73, 74	(Built in Skin)
16	2	Timers	WFF		Electronic (Chucks or Daves)

Micro PCM Stack Vector MMP-600

1	1	Programmer	Vector	PR-614
2	1	Timer	Vector	TM-615P
3	2	Digital Par. Mux	Vector	PD-629
4	3	Analog Mux	Vector	MP-601
5	1	Quad Filter & Amp	Vector	FL-619A
6	1	Formatter	Vector	FM-618
7	1	A-D Converter	Vector	AD-606-HS
8	1	Power Supply	Vector	PX-628

APPENDIX B

HAMAMATSU PCD IMAGE SENSOR TECHNICAL DATA

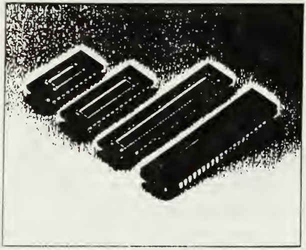
HAMAMATSU
TECHNICAL DATA

PCD LINEAR IMAGE SENSORS S2300 SERIES

(50μm × 5.0 mm Aperture Size)

The S2300 series PCD linear image sensors are monolithic self-scanning photodiode arrays designed specifically for applications in multichannel spectroscopy. The scanning circuit is constructed by a Plasma-Coupled Device (PCD). This scanner is a novel bipolar static shift register and is operatable with a single low power supply voltage. PCD image sensors feature low spike noise, large sensitive areas, and high UV light sensitivity that allow high S/N ratios even in low-light-level detection applications.

The photodiodes of the S2300 series are arrayed in a row with 50 μm center to center spacing and 5.0 mm height. The sensitive area is twice as large as the S2301 series, thus well suited for low-light-level detection requiring high sensitivity. Three different numbers of photodiodes, 256 (S2300-256Q), 512 (S2300-512Q), and 1024 (S2300-1024Q) are available. Quartz glass is the standard window material. (Fiber optic window types are also available.)



From left: S2300-256Q, S2300-512Q, S2300-1024Q, S2300-1024F

FEATURES

- Wide photosensitive area; 50 μm × 5.0 mm
- Bipolar-type image sensor
- Wide operating frequency; DC to 2MHz
- Operatable with low voltage, single power supply
- Logic inputs (start pulse, shift clocks) are TTL compatible (open collector type)
- Low capacitive switching noise
- High UV sensitivity
- High output linearity and uniformity
- Low dark current and high saturation charge allow a long integration time for a wide dynamic range even at room temperature.

IMAGE SENSOR STRUCTURE

The PCD linear image sensor is a monolithic integrated circuit constructed with photodiode arrays, PCD shift register and switching transistors for addressing the photodiodes. Fig.1 shows the equivalent circuit.

The PCD shift register is a static type self-scanner that transfers an addressing pulse along the chain driven by a synchronized three phase clock. Each output pulse (negative polarity) from the PCD shift register is then led to the base electrode of each p-n-p switch in the video circuit. Photodiodes act as the emitters in these lateral transistors, and operate in the charge storage mode. Therefore the outputs are proportional to the product of the illumination intensity and repeated scanning period.

As shown in Fig.1, the equivalent circuit of S2300 series is very simple, no dummy photodiode is necessary and the signal is available from only one row as a sequential output. Furthermore the uniformity and purity of the signal is high, making it possible to measure the light intensity more accurately with a simple peripheral driving and signal processing circuit.

Fig.2 shows the sensor geometry. The photodiodes consist of diffused p-type regions in n-type silicon substrates. The charges generated in these two regions are collected and stored on the associated P-N junction's capacitance during the integration period. The p-type diffused region is specially processed to have high sensitivity in the UV region and lower dark leakage current.

Figure 1: Equivalent circuit

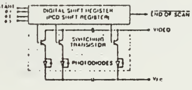
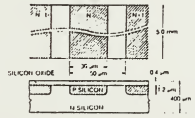


Figure 2: Sensor geometry



MAXIMUM RATINGS

Supply Voltage	10V
Operating Temperature	−30 to +85°C
Storage Temperature	−40 to +125°C

ELECTRICAL CHARACTERISTICS (at 25°)

Parameters	Symbols	S2300-256Q Min.	S2300-256Q Typ.	S2300-256Q Max.	S2300-512Q Min.	S2300-512Q Typ.	S2300-512Q Max.	S2300-1024Q Min.	S2300-1024Q Typ.	S2300-1024Q Max.	Units
Supply Voltage	Vcc	3	5	7	3	5	7	3	5	7	V
Driving Phase			3			3			3		phase
Shift Pulse Voltage*1	Vsh (H)	4.0	5	5.5	4.0	5	5.5	4.0	5	5.5	V
	Vsh (L)			0.8			0.8			0.8	V
Start Pulse Voltage	Vs (H)		Vcc			Vcc			Vcc		V
	Vs (L)			0.8			0.8			0.8	V
Operating Frequency	f	DC		2	DC		2	DC		2	MHz
Photodiode Capacitance	Cp		8			8			8		pF
Video Line Capacitance	Cv		25			40			50		pF
Power Consumption*1	P		30			30			30		mW
Photodiode Dark Current*1	Id		4	10		4	10		4	10	pA

*1: At Vcc = 5V

OPTICAL CHARACTERISTICS

Spectral Response (20% of peak)	200 to 1000 nm
Wavelength of Peak Response	600 nm
Saturation Exposure Esat*1	50 mlux·sec.
Saturation Charge Qsat	37 pC
Sensitivity Uniformity*2	within ± 5%

*1: At Vcc = 5V
*2: 50% of saturation, excluding first element

Figure 3: Typical spectral response

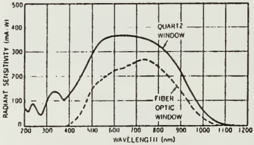


Figure 4: Output charge vs. exposure

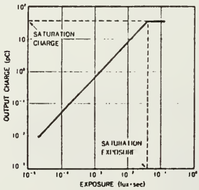
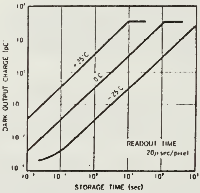
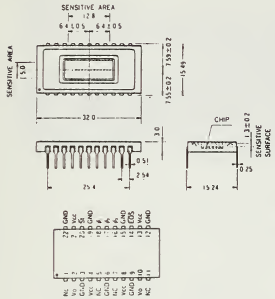


Figure 5: Dark output charge vs. storage time temperature dependency

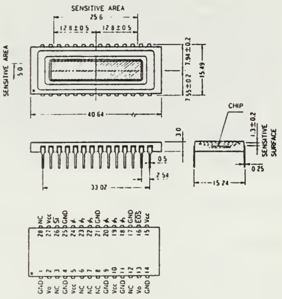


DIMENSIONAL OUTLINES AND PIN CONNECTIONS (Dimensions in millimeters)

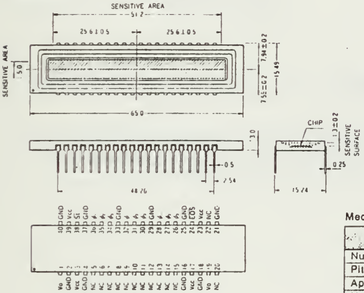
S2300-256Q



S2300-512Q



S2300-1024Q



Symbols	Functions
Vo	Video Output Two Vo are connected inside the element.
Vcc	Power Supply Voltage
GND	Ground (0V)
$\overline{St}$	Start Pulse Input (TTL compatible)
φ	Clock Pulse Input (TTL compatible)
$\overline{EOS}$	End of Scan Negative C-MOS compatible. Obtainable at the clock timing just after the last element is scanned.
NC	No Connection This should be grounded.

Mechanical Specifications

Parameters	S2300-256Q	S2300-512Q	S2300-1024Q
Number of photodiodes	256	512	1024
Pitch (μm)	50		
Aperture (μm)	50 × 5000		
Number of pins	22	28	40
Window material*	Quartz		
Net weight (g)	4	5	8

*Fiber optic window available.

DRIVING AND AMPLIFIER CIRCUIT

The clock pulse timing and circuit parameter requirments for driving the S2300 series PCD image sensor are shown in Fig.6 and Fig.7. To operate the PCD shift register requires a start pulse to initiate the scan and three phase clock to drive sequentially. The polarity of the start pulse has to be negative and the clock pulses must be positive. These pulses are TTL compatible. The start pulse needs at least 500 ns duration time and a minimum of 200 ns overlap with the clock pulse ϕ_1 to start the scan. It is not always necessary to overlap clock pulses each other, but if a gap of more than 100 ns is presented, scanning will disable.

An open collector type TTL is used to drive the PCD shift register. The voltage level of the start and shift pulse are determined by Vs and Vsh respectively. To provide stable operation of the shift register, it is necessary to select an optimized injection current controlled by resistances R_1 and R_2. Typical values of these driving parameters are shown in Fig.7 and the electrical characteristics table.

To detect low light levels with good linearity, video current integration with a charge-amplifier is recommendable. Fig.7 shows this type of signal extraction with this circuit, the charge-amplifier is reset to ground prior to address each photodiode multiplex switch. When the switch is closed, signal charge flows into capacitors in the integration circuit. The output wave form is a box car shape.

Figure 6: Timing diagram (3-phase drive)

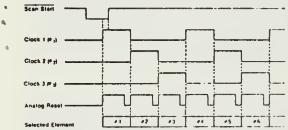
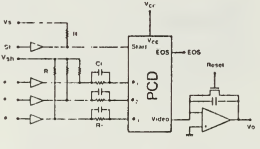


Figure 7: Driving and amplifier circuit



Vcc, Vsh and Vs are operatable with the same supply voltage.
Typical values of the parameters
CE: 2 nF, R1: 5.6 kΩ, R2: 470 Ω

RELATED DEVICES

•S2301, S2304 Series PCD Linear Image Sensors

Hamamatsu provides other sensor geometries for the PCD linear image sensors. The S2301 series has photodiodes of 50 μm × 2.5 mm and the S2304 series has those of 25 μm × 2.5 mm. Types with 128 to 1024 photodiodes are available.

•Driver/Amplifier Circuits for PCD Linear Image Sensors

Driver/amplifier circuits for PCD image sensors are available. These circuits need only a start pulse, master clock pulse, + 5V and ± 15V power supply to drive the PCD image sensor. The video output is a voltage output processed by a charge-amplifier. Pulse generator for these driver/amplifier circuits and data processing unit for A/D conversion are also available.

HAMAMATSU

HAMAMATSU PHOTONICS K.K., Solid State Division
1126, Ichino-cho, Hamamatsu City, 435 Japan, Telephone: 0534/34 3311, Fax: 0534/35-1037, Telex 4225-185

U.S.A.: Hamamatsu Corporation: 360 Foothill Road, P.O. Box 6910, Bridgewater, N.J. 08807-0910, Telephone: 201-231-0960, Fax: 201-231-1539
W.Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-8036 Herrsching am Ammersee, Telephone: 08152-375-0, Fax: 08152-2658
France: Hamamatsu Photonics France: 49/51 Rue de la Vanne, 92120 Montrouge, Telephone: (1) 46 554 758, Fax: (1) 46 55 36 65

JUL/87
T-2000 Printed in Japan

APPENDIX C

HAMMAMATSU DRIVER AMPLIFIER TECHNICAL DATA

OPERATING INSTRUCTIONS FOR EVALUATION BOARD

HAMAMATSU PHOTONICS K.K.
SOLID STATE DIV.

SD29-890717-0051201.

OPERATING INSTRUCTIONS FOR EVALUATION BOARD

GENERAL

This is low noise driver/amplifier circuit for Hamamatsu PCD Image Sensors (S2300-512Q,-512F).
The PCD image sensor is a monolithic self-scanning photodiode array. Its scanning circuit is constructed by Plasma-Coupled Device(PCD).
This driver/amplifier circuit provides a scanning pulse "Start" and a three phase clock " ϕ 1, ϕ 2, ϕ 3" to drive the PCD image sensor, and includes a charge-amplifier to output the video signal "Video Data" in the charge integration mode.

FEATURES

- Simple operation; a start pulse, a master clock pulse, +5V and ± 15V required.
- Low noise configuration.
- Structure allows for easy cooling and optical alignment.

SPECIFICATIONS

INPUTS ; Supply voltage: + 5 Vdc at 150mA
+15 Vdc at 25mA
-15 Vdc at 25mA

Start: TTL pulse, positive level sensitive. Minimum duration 500 nsec. Used to initialize the circuit and initiate the shift register in the PCD image sensor.

CLK: TTL pulse, rising edge sensitive. Maximum frequency 250 KHz. Used to syncronize the circuit and the shift register in the PCD image sensor.

OUTPUTS ; Trigger: LS-TTL compatible, positive pulse.
Available as a start signal for S/H and A/D conversion (optional).

$\overline{\text{B-EOS}}$: HS-CMOS compatible, negative pulse.
Available immediatly after scanning at the last pixel is completed.
Can be used as end of A/D aquisition.

Video Monitor: Negative voltage output.
This output is the integrated PCD video current signal.

Video Data: Positive voltage output.
It is the processed signal of the "Video Monitor".

SETUP PROCEDURE

Setup for the evaluation system is shown in Figure 1.

1) Power supply connection

Power, as specified under specifications, must be supplied to the driver/amplifier citcuit inputs.

2) Pulse generator connection

The "Start" pulse and the "CLK" pulse, as specified under specifications, must be supplied to the driver/amplifier circuit inputs. (C2335 "Hamamatsu Pulse Generator" available and can be connected to the two timing inputs respectively.)
The integration time is preset by the "Start" pulse interval while the readout time of each pixel is preset by a "CLK" frequency.

3) Oscilloscope connection

The "Start" pulse input (from C2325 or other clock) is connected both to the C2325 board and to the EXT. TRIG. input of the oscilloscope.
The "Video Data" signal output is the connected to the input of the oscilloscope.

4) S/H and A/D converter connection (optional)

The "Trigger" pulse output can be used as the logic input of S/H and A/D converter. The "Video Data" signal output is then connected to the analog input of the S/H.

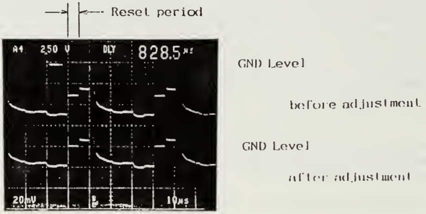
ALIGNMENT PROCEDURE

The driver/amplifier circuit assembly is shown in Figure 2.

REMARK: Use an oscilloscope to monitor the "Video Monitor" or the "Video Data" signal output without any light being illuminated on the photodiode array.

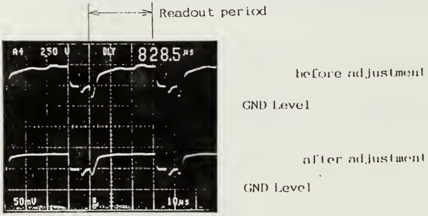
1) Zero level adjustment 1:

Adjust VR2(100K Ω) until the reset level comes to oscilloscope ground level.



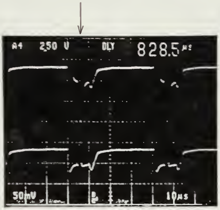
2) Fluctuation (caused by Power supply) cancellation adjustment:

Adjust VR3(1K Ω) until the fluctuation of the "Vedeo Data" signal is minimized.



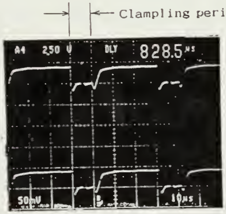
3) Switching noise cancellation adjustment:

Adjust VR1(10K Ω) until the amplitude of the spike noise is minimized.



4) Zero level adjustment 2:

Adjust VR4(10K Ω) until the clampling level comes to oscilloscope ground level.



REMARKS

If the evaluation system is not operated, regularly check the following items:

1) Are the "Start" pulse and the "CLK" pulse supplied to the driver/amplifier circuit inputs as prescribed under specifications ?

2) Is the scanning pulse "$\overline{\text{Start}}$" supplied to the PCD image sensor ?

3) Is the high level of the three phase clock (ϕ 1, ϕ 2, ϕ 3) according to "Figure 3 Timing Diagram" ?

4) Is the "$\overline{\text{EOS}}$" pulse obtained from the pin of the PCD image sensor ?

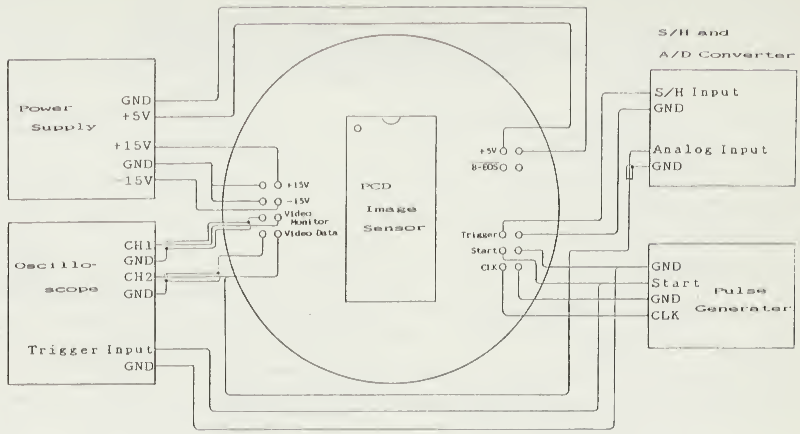
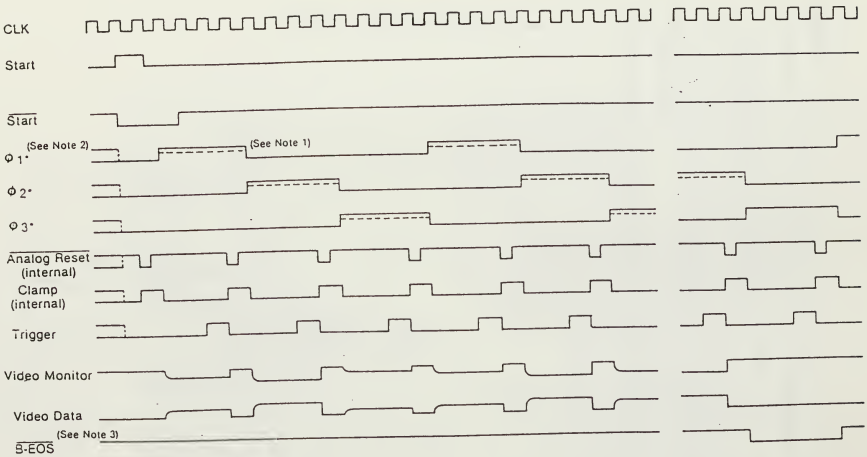


Figure 1 Setup for Evaluation System



Note 1: Solid lines are "PCD-OFF", broken lines "PCD-ON".
2: Pulse width of a three phase clock "Φ 1, Φ 2, Φ 3" is 4 times of a "CLK" period.
3: This $\overline{\text{B-EOS}}$ syncronizes to the next "clock" right after scanning of the last element (of PCD Image Sensors). That is, regarding 128 and 512 elements types, the last element is scanned by Φ 2 and $\overline{\text{B-EOS}}$ is obtained by the timing of Φ 3. And regarding 256 and 1024 elements types, $\overline{\text{B-EOS}}$ is obtained by Φ 2.

Figure 3 Timing Diagram

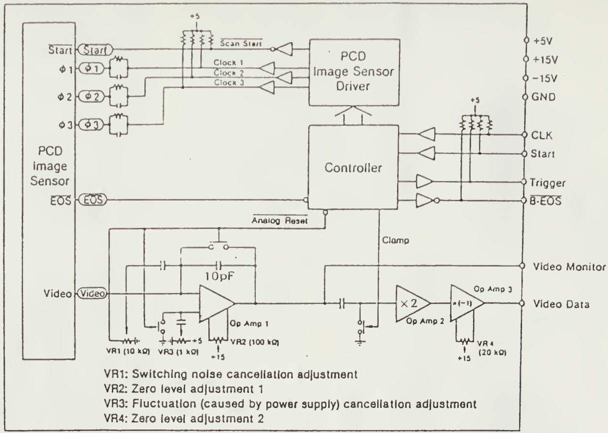
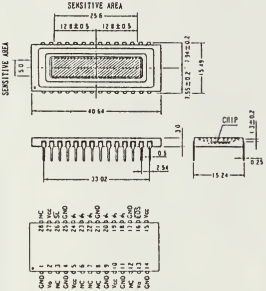


Figure 4 Circuit Configuration

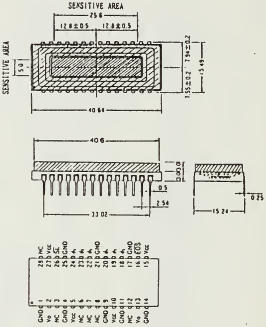
Appendix 1

Pin configurations and package outlines of PCD Image Sensor are shown in Figure A-1

S2300-512Q



S2300-512F



Symbols	Functions
Vo	Video Output Two Vo are connected inside the element.
Vcc	Power Supply Voltage
GND	Ground (0V)
$\overline{SI}$	Start Pulse Input (TTL compatible)
ϕ	Clock Pulse Input (TTL compatible)
$\overline{EOS}$	End of Scan Negative C-MOS compatible. Obtainable at the clock timing just after the last element is scanned.
NC	No Connection This should be grounded.

Parameters	S2300-512Q	S2300-512F
Number of photodiodes	512	
Pitch (μm)	50	
Aperture (μm)	50 x 5000	
Number of pins	28	
Window material	Quartz	Fiber optic plate
Net weight	5g	13.6g

Figure A-1 Pin Configurations and Package Outlines of PCD Image Sensor

Appendix 2

Circuit configuration of the pulse generator is shown in Figure A-2

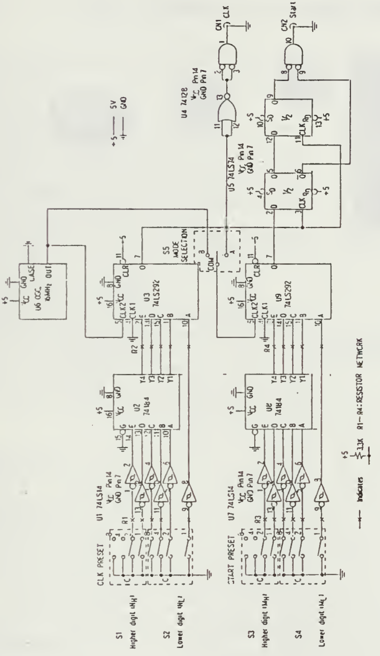


Figure A-2 Circuit Configuration of Pulse Generator

APPENDIX D

IMAGE INTENSIFIER TECHNICAL DATA

F4144
F4145
F4150

Proximity Focused Channel Intensifier Tubes with Dual Microchannel Plates

Image Intensifiers

Features:

- Lightweight
- Short Length
- Ruggedized Construction
- Uniform Brightness
- Zero Distortion
- High Gain
- Fast Response
- Gatable
- Non-Blooming
- Photon Counting

ITT Type Number	Format	Spectral Response (Note 1)
F4144	18mm	S-20
F4145	25mm	S-20
F4150	40mm	S-20

ITT proximity focused channel intensifier tubes with dual microchannel plate are miniaturized, very high gain, image intensifiers. All of these tubes utilize two microchannel plates in cascade to provide very high electron gain for ultra low light level amplification. A basic tube consists of a photocathode, two microchannel plates in cascade, and an output phosphor screen. The tube envelope is of a metal-ceramic construction with a glass, fiber optic or other input window and a plano-plano fiber optic output window. All tubes of this type are gateable. The F4144 is capable of being gated on, within 5 nanoseconds after application of the gate pulse, by switching the inherently low cathode to microchannel plate (MCP) input voltage.

GENERAL CHARACTERISTICS

Photocathode:
- Spectral response (Note 1) S-20
- Peak response .... 450-550 nanometers
- Window (Note 2) .... plano-plano glass

Phosphor:
- Spectral response (Note 3) .... P-20, aluminized
- Peak response .... 510-570 nanometers
- Window .... plano fiber optic

Focusing method .... Proximity
Operating position .... Any
Maximum Temperature (non-operating) .... 65°C
Magnification 1:1

TYPICAL PERFORMANCE CHARACTERISTICS (for specified voltage)

Supply voltages DC (Note 4)
- Phosphor-to-MCP .... 5 to 6 KV
- MCP .... 1000-1800 Volts
- Photocathode to MCP .... 150 to 200 Volts

Cathode Luminous sensitivity:
- Typical .... 225 μa/lumen
- Minimum .... 175 μa/lumen

Luminous gain, variable (Note 5) .... 10^{4}-10^{6}
Maximum Light Level (Note 7) .... 5 X 10^{-4} footcandles
Resolution range (Note 6) .... 18-20 linepairs/mm
Equivalent brightness input (Maximum) .... 2 X 10^{-11} lumens cm²

Engineering and applications assistance for the tube types listed above may be obtained by contacting Electro-Optical Products Division.

NOTICE: AN EXPORT LICENSE IS REQUIRED FOR SHIPMENT OF THIS PRODUCT OUTSIDE OF THE USA.

REV 6/86 ELECTRO-OPTICAL PRODUCTS DIVISION ITT

NOTE 1 Other photocathodes available on special order, include the S-1, to provide detection and conversion of 1.06μ signals, and CsTe, CsI cathodes for special UV applications.

NOTE 2 Fiber optics, quartz, MgF_2, or other materials available on special order.

NOTE 3 Other phosphors available on special order.

NOTE 4 Power Supplies can be an integral part of the tube assembly. Gateable and DC power supplies are available as separate units.

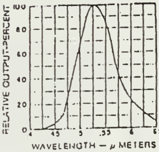
NOTE 5 Defined as the ratio of the total luminous flux from the phosphor screen to the total luminous flux incident on the photocathode from a standard 2,854° K tungsten lamp, and measured with a photometer as ft L/ft c with an input level of $1 X 10^{-6}$ ft-c incident on the photocathode. The ITT proximity focused channel intensifier tube provides a variable tube gain by varying the microchannel plate voltage.

NOTE 6 There is no degradation of resolution from center-to-edge of screen. Resolution is measured with $5 X 10^{-4}$ footcandles on the photocathode to determine limiting, or 5 per cent MTF levels with a 100 per cent contrast target.

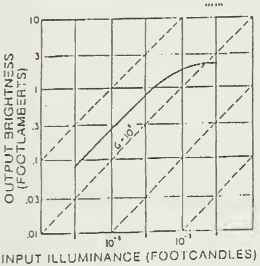
NOTE 7 For continuous operation; this value may be several orders of magnitude higher for pulsed operation.

NOTE 8 Maximum output brightness that can be achieved from these tubes will range from 1-2 Footlamberts under D.C. operating conditions.

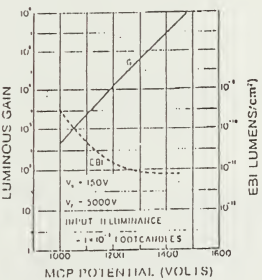
SPECTRAL OUTPUT
P-20 PHOSPHOR

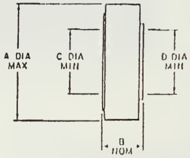


TYPICAL SATURATION CURVE
OF PROXIMITY FOCUSED
MICROCHANNEL WAFER TUBE

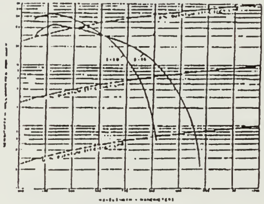


TYPICAL GAIN CHARACTERISTICS
OF PROXIMITY FOCUSED
MICROCHANNEL WAFER TUBE





TYPICAL ABSOLUTE
SPECTRAL RESPONSE CHARACTERISTICS



Dimensional Data	18mm F4144	25mm F4145	40mm F4150	Units
A Maximum diameter (with potting)	45	53	71	mm
B Length (nominal)	21	21	24	mm
C Useable Photocathode Aperture	18	25	40	mm
D Useable Screen Aperture	18	25	40	mm
Potted Weight	60	105	215	grams

ELECTRO-OPTICAL
PRODUCTS DIVISION
3700 East Pontiac Street
P.O. Box 3700
Fort Wayne, Indiana 46801

-DATA SHEET 1-

-PROXIMITY FOCUSED CHANNEL INTENSIFIER TUB

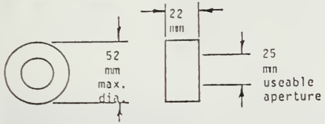
TUBE S/N XXII 0966

TUBE TYPE F4145

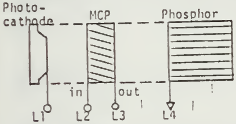
CsTe/Q/P20/FO

DATE 09/28/89

1.0 OUTLINE DRAWINGS



2.0 ELECTRICAL SCHEMATIC



3.0 LEAD CONNECTIONS

LEAD	COLOR	ELEMENT	
1	Blue	Photocathode	(neg.)
2	Red	MCP Input	(neg.)
3	Orange	MCP Output	(neg.)
4	Yellow	Phosphor	(ground)

4.0 TYPICAL OPERATING VOLTAGES *

Cathode to MCP input	180	volts
MCP input to MCP output	1670	volts
MCP output to Phosphor	5K	volts
* voltages for	30 ke-	gain

4.1 MAXIMUM OPERATING VOLTAGES **

Cathode to MCP input	180	volts
MCP input to MCP output	1700	volts
MCP output to Phosphor	5K	volts
** voltages for	40 ke-	gain

4.2 Use with power supply
Model # 200057 S/N 0110

Power supply set so that when Vcontrol = 10.0 V, Vmcp = 1700 V. The product of the photocathode current and the MCP gain must not exceed 0.1 uA/cm^2.

5.0 CATHODE SENSITIVITY

N/A ua/lumen
(see sensitivity curve)

6.0 RESOLUTION

N/A lp/mm
@ ______ MCP volts

7.0 LUMINOUS GAIN

N/A

8.0 GAIN UNIFORMITY

11 %
@ 40 ke- gain

9.0 EQUIVALENT BACKGROUND INPUT

N/A lumens/cm^2
@ ______ gain

-PROXIMITY FOCUSED CHANNEL INTENSIFIER TUBE-

Tube S/N XXII 0966 Tube Type F4145 Date 09/28/89

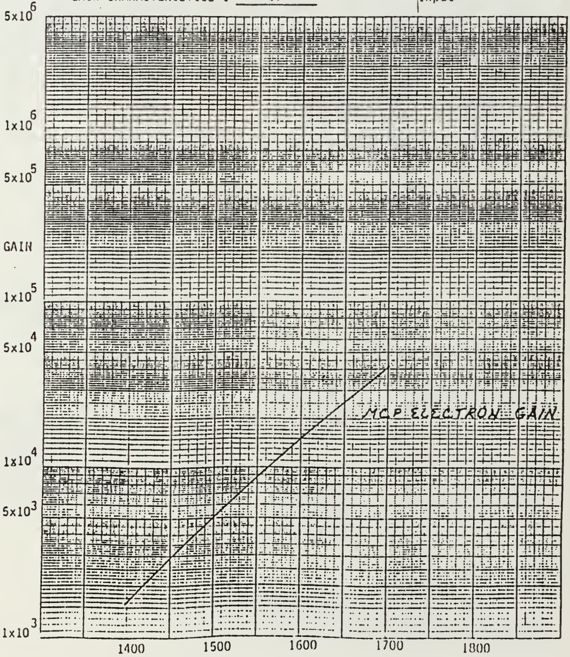
MCP Conductivity 3.3×10^{-6} amps @ 1K volts

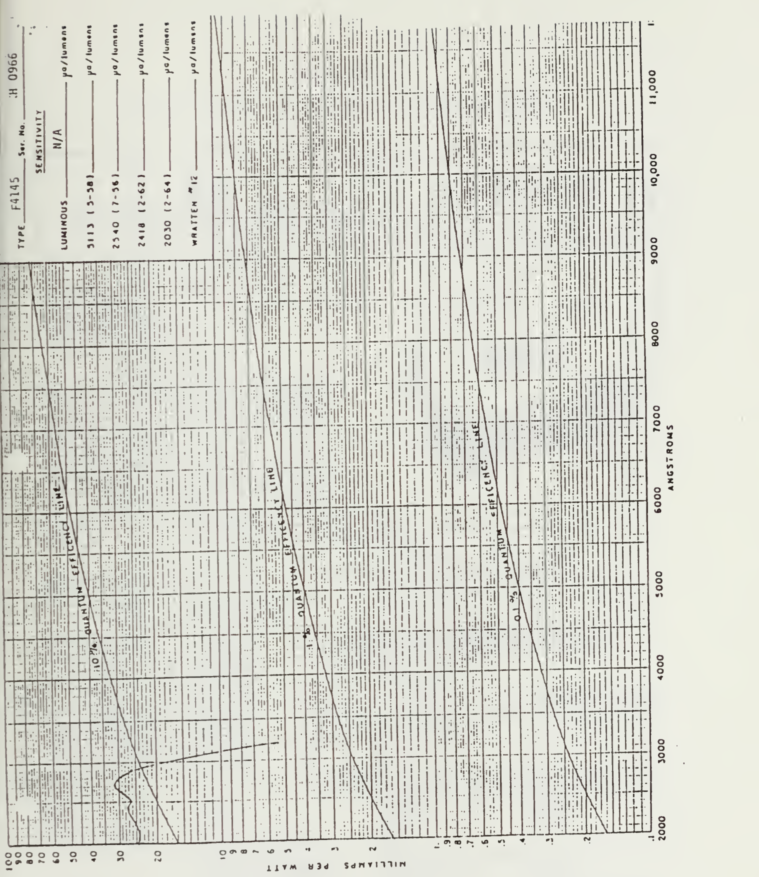
Photocathode Sensitivity N/A ua/L @ ______ Lumens

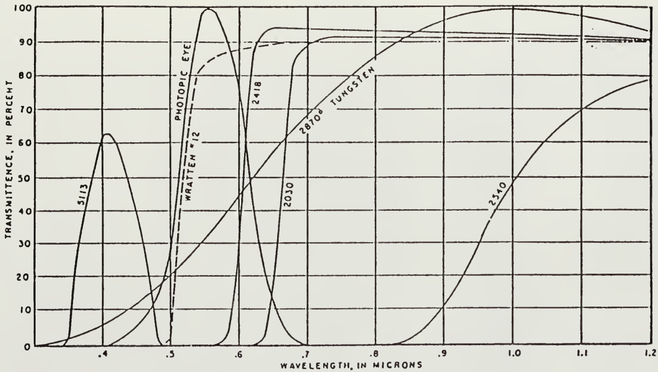
Photocathode Type/Window CsTe, Q Phosphor Type P-20

Photocathode Voltage 180 Phosphor Voltage 5K

GAIN CHARACTERISTICS @ UV Input




TYPE F4145 Ser. No. H 0966
SENSITIVITY
LUMINOUS N/A μa/lumens
5113 (5-58) μa/lumens
2540 (7-56) μa/lumens
2418 (2-62) μa/lumens
2030 (2-64) μa/lumens
WRATTEN #12 μa/lumens
10% QUANTUM EFFICIENCY LINE
1% QUANTUM EFFICIENCY LINE
0.1% QUANTUM EFFICIENCY LINE
2000 3000 4000 5000 6000 7000 8000 9000 10,000 11,000
ANGSTROMS
MILLIAMPS PER WATT



The standard luminous sensitivity is the response of the photocathode (in microamperes per lumen) to a tungsten lamp operating at 2870°K. The various numbered sensitivities are the response of the photocathode when Corning filters (filter numbers are four digits; dashed, three digit numbers in parentheses are a color specification number) of half stock thickness are interposed between the 2870°K lamp and the photocathode. Plotted above are the transmittance, in percent, of the filters, and the spectral distribution, in relative units, of 2870°K tungsten. Also shown are the photopic eye response and the transmission of a Wratten #12 filter.

APPENDIX E

AYDIN VECTOR TRANSMITTER TECHNICAL DATA

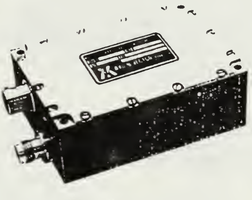
AYDIN VECTOR	T-100-TV Series UHF Video Transmitters

- Available In 2, 5 and 8 Watts Minimum Power
- Video Response
- Wideband Deviation
- Internal Power Line Regulator
- Internal Output Isolator
- Meets IRIG 106-80 Standards

The Vector T-100-TV Series are solid-state, crystal stabilized, true FM telemetry transmitters capable of transmitting analog or digital multiplex signals. These transmitters are designed for extremely reliable operation when subjected to the severe environmental flight conditions of missiles, space vehicles and aircraft.
The internal modules (modulator, series regulator, power amplifier, multipliers and filters) are housed in separate machined enclosures to maximize RF isolation. Components are derated from the manufacturers rated values and all semiconductors undergo 100 Hrs. burn-in at 100°C. to insure reliable operation while meeting the specified output power requirements under worst case conditions.

ELECTRICAL SPECIFICATIONS

Output	
Frequency Range:	1710 to 1850 MHz 1435-1540 MHz (S band optional)
Frequency Stability:	±0.003%
Power Output:	
T-102-TV	2 watts min.
T-105-TV	5 watts min.
T-108-TV	8 watts min.
Antenna Compatibility	
Output Impedance:	50 ohms
VSWR (load)	1.5:1
Open/Short Protection:	Yes, Internal Isolator
Harmonic/Spurious Response:	IRIG 106-80
Modulation	
Type:	True FM
Sense:	Positive
Input Impedance:	75 ohms
Frequency Response:	10 Hz to 6 MHz ±1.5 dB (to 10 MHz optional) Optional pre-emphasis In accordance with CCIR-405)
Deviation:	±6 MHz/V rms (increased sensitivity optional)
Deviation Linearity:	2.0% max BSL for ±6 MHz deviation
Modulation Distortion:	2.0% max for ±6 MHz deviation
Incidental FM:	±10 kHz
Incidental AM:	2% max
Modulation Return:	Modulation return common to case



Power	
Voltage:	28 ±4 Vdc
Current:	
T-102-TV	1.0 A max
T-105-TV	2.0 A max
T-108-TV	2.5 A max
Reverse Polarity Protection:	Yes
Power Return:	Power return common to case

ENVIRONMENTAL SPECIFICATION

All performance specifications will be met under the following conditions.

Temperature:	
T-102-TV	−25°C to +85°C baseplate
T-105-TV	−25°C to +80°C baseplate
T-108-TV	−25°C to +70°C baseplate extended range optional
Vibration: Sine	20g, 20 to 2,000 Hz, 3 axis
Shock:	50g for 11 msec ½ sine, 3 axis
Acceleration:	100g, 3 axis
Altitude:	Unlimited
Humidity:	90% RH
EMI:	Complies with IRIG 106-80

MECHANICAL SPECIFICATIONS

Dimensions:	See Dwg.
Weight:	16 ounces/0.45 kg max
Volume:	11.5 Cu. Inches/188548.0 Cu. mm less connectors
Connectors:	
Power	Bendix PT1H-8-4P males with Bendix PT06A-8-4S
MOD Input	SMA .250-36 UNS-2B males with SMA male
RF Output	TNC 7/16 - THD males with TNC Male

Pin Connections:	A) +28 Vdc B) N/C C) Power RTN D) Chassis Gnd

OPTIONS

Frequency Range:	S and L-band, specify center frequency
Frequency Response:	10 Hz to 10 MHz.
Pre-emphasis:	In accordance with CCIR-405
Deviation Sensitivity:	Higher sensitivity available
Modulation Type:	TTL compatibility
Extended Temp:	−40°C to +85°C

QUALITY CONTROL AND PRODUCT ASSURANCE

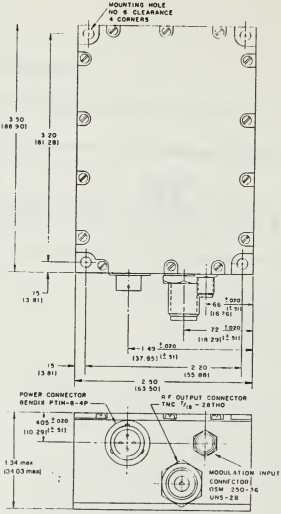
The Vector T-100-TV Series transmitter is manufactured under strict Quality Control procedures in accordance with the requirements of MIL-Q-9859A. Additionally, all semiconductors and integrated circuits are used in the T-100-TV are subjected to intensive component pre-conditioning procedures. Each assembled unit is fully tested to a comprehensive Acceptance Test procedure which includes full performance testing at the thermal extremes.

Vector has participated in numerous "hi-rel" aerospace programs which have required exhaustive component screening, preconditioning and selection procedures. These "hi-rel" procedures or specific customer generated requirements can be invoked in the manufacture of the T-100-TV series transmitters if necessary.

ORDERING INFORMATION

When ordering specify series number and exact operating frequency in megahertz. For special applications or additional information, contact Aydin Vector or the nearest sales representative.

Outline Drawing
T-100TV



Dimensions in inches (mm)

Bulletin 27125/Rev.1/5/85/2M/Printed in USA

AYDIN VECTOR DIVISION

NEWTOWN INDUSTRIAL COMMONS • P.O.Box 328, NEWTOWN, PA 18940-0328 • (215) 968-4271 • TWX: 510-667-2320 • FAX: (215) 968-3214

APPENDIX F

POWER SUPPLY TECHNICAL DATA

RSI

RESEARCH SUPPORT INSTRUMENTS, INC.
10810 BEAVER DAM ROAD, COCKEYSVILLE, MARYLAND 2103
PHONE 301-785-6250 FAX 301-785-1228

Item No. 0001AK

LOW VOLTAGE POWER SUPPLY

RSI MODEL 428-211

The RSI Model 428-211 is a low voltage power supply which operates from a nominal +28VDC input. The output of the unit is +5V and provides up to 1000mA. A current limited output monitor is provided in parallel with the output voltage.

The input is series diode protected against inadvertent reversal of the input power lines. Heat sinking of the case is recommended for full power operation.

SPECIFICATIONS:

Input Voltage...............+24VDC to +34VDC
Input Current................70mA (no load)
500mA (1000mA load)
Output Voltage...............+5V (+-5%)
Output Ripple................< 50mV
Output Spikes................< 75mV
Efficiency...................>30% at full load
Converter Frequency..........Nominal 10KHz
Operating Temperature........-20 C to +70 C
Storage Temperature..........-40 C to +85 C
Line Regulation.............. .02%/V (no load)

MECHANICAL:

Dimensions...................1.0 in.X 3.0 in.X 3.5 in.
Weight.......................300 grams
Mounting.....................Four (4) size six clearance holes
Connector....................Cannon DAM 15P

OPTIONS:

Voltages other than +5V upon request.
Potting or conformal coating upon request.

Research Support Instruments

Test Report

Low Voltage Power Supply

Model Number 428-211

Serial Number 122503

Voltage Input 28.0 V

Input Voltage (V)	Input Current (mA)	Output Voltage (V)	Output Current (mA)	Monitor Output (V)	Output Ripple (mV)
28	38	5.24	0	5.24	20
28	74	5.23	100	5.23	20
28	108	5.21	200	5.21	25
28	147	5.20	300	5.20	20
28	187	5.18	400	5.18	25
28	224	5.17	500	5.17	25
28	259	5.16	600	5.16	30
28	297	5.14	700	5.14	25
28	337	5.12	800	5.12	25
28	380	5.11	900	5.11	30
28	420	5.09	1000	5.09	30

Notes:

1 Unit should be well heatsunk.
2 Unit loses regulation at 24.2 V input.

Signature Chris Weisner

Date 12-7-89

Disk:wptest File:wp122503.rma

RESEARCH SUPPORT INSTRUMENTS, INC.
10610 BEAVER DAM ROAD, COCKEYSVILLE, MARYLAND 21030
PHONE 301-785-6250 FAX 301-785-1228

Item No. 0001AL

DUAL TRACKING LOW VOLTAGE POWER SUPPLY

RSI MODEL 441-193

The RSI Model 441-193 is a dual tracking low voltage power supply which operates from a nominal +28VDC input. The outputs of the unit are complementary (+15V and -15V) voltages, each capable of providing 400mA, which track each other under various loads. A current limited output monitor is provided in parallel with the output voltage.

The input is series diode protected against inadvertent reversal of the input power lines. Voltages other than 15V can be supplied upon request. Heat sinking of the case is recommended for full power operation.

SPECIFICATIONS:

Input Voltage	+24VDC to +34VDC
Input Current	70mA (no load) 840mA (400mA load)
Output Voltage	+15VDC @ 400mA -15VDC @ 400mA
Output Ripple	Less than 25mV
Output Spikes	Less than 150mV
Efficiency	60% at full load
Converter Frequency	Nominal 10.5KHz
Operating Temperature	-20 C to +70 C
Storage Temperature	-40 C to +85 C
Line Regulation	0.02%/V (no load)
Load Regulation	0.01%/V (400mA load)

MECHANICAL:

Dimensions	1.0 in.X 3.0 in.X 3.5 in.
Weight	212 grams
Mounting	Four (4) size six clearance holes
Connector	Cannon DAM-15P

OPTIONS:

Voltages other than 15V upon request.
Potting or conformal coating upon request.

Research Support Instruments

Test Report

Low Voltage Power Supply

Model Number 441-193

Serial Number 122508

Voltage Input 28.0 V

Input Current (mA)	Output Voltage (V) +	Output Voltage (V) −	Output Current (mA) +	Output Current (mA) −	Monitor Output (V) +	Monitor Output (V) −	Output Ripple (mV) +	Output Ripple (mV) −
47.7	15.0	15.0	0	0	15.0	15.0	10	10
290	15.0	13.1	0	300	15.0	14.9	10	10
290	13.0	15.0	300	0	14.9	15.0	10	10
536	13.1	13.1	300	300	15.0	14.9	10	10
716	14.9	14.9	400	400	14.9	14.9	10	10

Notes:

1 Unit should be well heatsunk.
2 Unit loses regulation at 25.0 V input.

Signature For [signature]

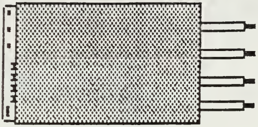
Date 11/02/89

Disk:wptest File:wp122508

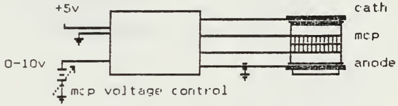
HV POWER SUPPLY GEN II

Grounded Anode

Gen II intensifiers



Model: 200057



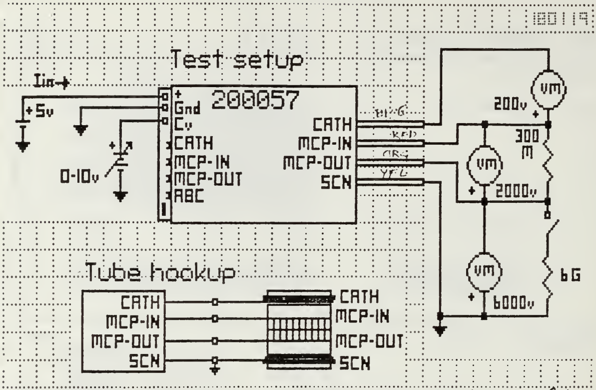
- o Grounded Anode Gen II outputs
- o Adjustable cathode, mcp-in, mcp-out, and ABC level
- o Ext MCP voltage control
- o Ext resistor select - ABC max limit for desired tube dia

cathode voltage	min adjustable range	100 to 240	vdc
	cathode series resistance	1	Gohm
mcp-in voltage	voltage controllable	to 2kv max	vdc
	max load current	20	uA
mcp-out voltage	adjustable	3000 to 6500	vdc
	brightness current limit	.05 to 5	uA
anode output	ground return potential	0	vdc
temperature	operational	- 55 to + 70	C
mechanical	4-40 inserts bottom surface corners		

190079

GBS	NAME Grounded Anode Gen II				DWG NUM 200057	
	SIZE A	BY GBS	DATE 07-27-86	SCALE N/A	REV B	SHT 1 OF 1

PS 200057 Test Data Sheet



Test Data at Delivery S/N : 010 Date : 7-13-87 By : [illegible]

Parameter	Data	Units
1. Cathode voltage @ no load	200	- VDC
Cathode voltage @ 1M	1.5	- VDC
2. Mcp-in voltage @ 300M @ Cv=10v	1700	- VDC
8v	1400	- VDC
6v	1100	- VDC
4v	700	- VDC
2v	270	- VDC
3. Mcp-out voltage @ no load	5500	- VDC
@ 1 uA load	5450	- VDC
4. Rabc set value	1.0	megohm
ABC adj pot set for I-limit of	1.0	uA
5. Input current @ +5vdc @ ss	87	mADC
6. Burn-in	48	hrs
7. Mechanical and visual	✓	check

90126

GBS	NAME PS 200057 Test Data Sheet			DWG NUM 200123	
	SIZE A	BY GBS	DATE 02-16-87	SCALE N/A	REV A	SHT 1 OF 1

Operation and Instructions
PS 200057 grounded anode standard GEN II

1.0 General

The model 200057 power supply is a small DC to DC converter which converts +5 vdc to multiple HV dc outputs for use by a Gen II image intensifier tube. The outputs are line regulated, and each is independently adjustable. The power supply circuitry is fully potted in an RTV encapsulant due to the high internal voltages generated, and due to the small size of the power supply.

Manufacturer : GBS Micro Power Supply
6155 Calle Del Conejo
San Jose, California 95120
408-997-6720

2.0 Power Supply Inputs

The following inputs are available and marked on the power supply.

1. Input voltage terminal	+5 +-.5 vdc
2. Input voltage return terminal (gnd)	
3. Voltage control terminal	0 to +10 vdc
4. Cathode output adj pot	
5. MCP-IN output adj pot	
6. MCP-OUT output adj pot	
7. ABC limit fine adjust pot	
8. Rsel resistor for gross ABC limit adj	

3.0 Output Connections

There are 4 output leads for connection to the image intensifier.

1. Cathode output	typically -175 vdc with respect to the MCP-IN output lead
2. MCP-IN output	typically -1500 vdc with respect to the MCP-OUT output lead
3. MCP-OUT output	typically -6000 vdc with respect to the screen output lead
4. Screen output	Gnd, and tied to the +5 return internally in the power supply.

4.0 Voltage Control

The MCP voltage applied to the intensifier, is provided by the MCP-IN and MCP-OUT outputs, which is termed the MCP voltage. This voltage can be remotely varied from approximately -400 vdc, (the oscillator drop out level), to -2000 vdc, by varying the voltage applied to the voltage control terminal from 0 to +10 vdc. The +10 vdc results in -2000 vdc MCP voltage. An open at the voltage control terminal results in a 0 vdc MCP voltage.

90123

GBS	NAME PS 200057 Operation & Instructions				DWG NUM 200122	
	SIZE A	BY DH	DATE 4-19-83	SCALE N/A	REV A	SHT 1 OF 3

FORM F15001

The -2000 vdc MCP voltage when the control voltage is at +10 vdc, can be lowered to near -400 vdc by adjusting the MCP-IN adjust pot counter clockwise. CW increases MCP voltage toward -2000. CCW reduces MCP voltage toward 0 vdc.

5.0 Cathode Output

The cathode output is adjustable via a trim pot. CW increases the output to -250 vdc. CCW reduces the output to -100 vdc. A cathode current limiting resistor (1 Gigohm) is internal in the power supply, and will drop the cathode voltage as excess tube cathode current is developed in high illumination conditions. When the cathode current, under these high current conditions, falls to approximately -3 vdc with respect to the MCP voltage, a diode in the power supply, shunts the 1 Gigohm limit resistor, with a 22 Megohm resistor, thereby extending the cathode current availabe, before eventual tube cutoff.
The cathode output is typically -175 vdc with respect to the MCP-IN output, but it is stacked on the other power supply outputs, so that with respect to ground, the potential on the cathode lead is approximately -8000 vdc. This high voltage is usually a source of trouble when operating the power supply, as leakage to gnd may often readily develop. This leakage will be treated by the power supply as ABC current, which is an instruction to the power supply to lower, or shut off the MCP-IN voltage. Caution is recommended in the testing of the power supply, and in the tube connections.

6.0 MCP-out Voltage

The MCP-out is the votage provided for the intensifier screen, and is -6000 vdc typically. This output is connected to the MCP-OUT intensifier lead. CW adjustment of the trim pot increases this voltage to -6500 vdc. CCW decreases the voltage to -3000 vdc. This high voltage is developed in the power supply by a stack of voltage doubler circuits. This multiplier circuit is resistor returned to gnd, so that any tube screen current flowing at any time, must pass through the resistor. A voltage is developed across the resistor, and is proportional to the tube screen current. The voltage developed, is compared to an ABC limit setting, and will shut down the MCP voltage to the tube, if the threshold level is reached.

7.0 ABC

The R-select resistor (externally available as Rsel), is used to sense the tube screen current as described in paragraph 6.0.
The power supply comparator for ABC, has a threshold level of 1 vdc and will shut down the MCP voltage when the Rsel voltage reaches this 1 vdc threshold. The choice of resistance for Rsel, then can determine at what tube current, shutdown is desired. Typically, Rsel is chosen as 1 Megohm, so that it allows ample current for normal tube use, but limits screen current to a maximum of 1 uA.

.90119

GBS	NAME PS 20057 Operation & Instructions				DWG NUM 200122		
	SIZE A	BY DH	DATE 4-19-88	SCALE N/A	REV A	SHT 1	OF 1

FORM F15001

The ABC trim pot allows fine resolution of the threshold voltage used by the shutdown comparator. CW increases the threshold to 1.0 vdc. CCW decreases the threshold voltage to 0 vdc. In this manner, the ABC pot can be used to fine tune the limit current circuitry for use as an automatic brightness control feature, (ABC).
The power supply has a 22 Megohm internal resistor in parrallel with the external Rsel.
At delivery, Rsel is set to 1 Megohm, and the ABC pot is adjusted for so that 1 uA of screen current reduces the MCP voltage 50%.

8.0 Mechanical, Leads

The power supply chassis is glass epoxy with TRV potting internal. There are 4 Mounting inserts on the base of the power supply, 4-40 inserts.
The output leads are silicone coated teflon insulated stranded wires, reated for 15kv.

9.0 Processing, Burn-in

Standard processing prior to delivery includes 24 hrs of operation unpotted, at 23C, at nominal output voltage levels, followed by 48 hrs of operation at 23C, at typical output voltage levels, followed by a final electrical performance test at 23C.
Other tests and burn-in environments may be conducted as specified by the customer purchase order.

10.0 Test Circuitry

Electorstatic voltmeters or equivalent high input impedance (> 300 Gigohm) divider probes are recommended when checking output voltage levels.
A dc voltage applied to Rsel can be used to simulate tube screen current for MCP shutdown verification. This voltage should not exceed 5 vdc, the input supply voltage.

90119

GBS	NAME PS 200057 Operation & Instructions				DWG NUM 200122		
	SIZE A	BY DH	DATE 4-19-88	SCALE N/A	REV A	SHT 3	OF 3

FORM F15001

APPENDIX G

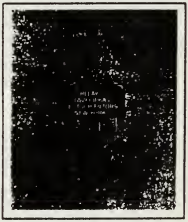
DEUTSCH RELAY TECHNICAL DATA

SERIES **DJ**

DJ2U D1 JCAS

1-12 14.53
13-49 13.03
50-99 12.15

The new five
crystal-case relay
with the most impressive list
of features in the industry.



CONSTRUCTION FEATURES:

Coil	The long thin Demi-J coil approaches the ideel shape; it delivers more empere-turns per wett. Thin-well bobbins increase efficiency and improve thermal conductivity — two assurances of long, relieble reley life.
Contects	The unique trapped pressure contect system ebsorbs the kinetic energy of the ermeture and damps the reactive forces which helps to reduce bounce and prevent crossover.
Size	Stenderd half-size crystal-case.
Seel	Hermetic; less than 1 x 10[?] cc/sec.
Weight	0.35 ounce maximum.

PERFORMANCE DETAILS:

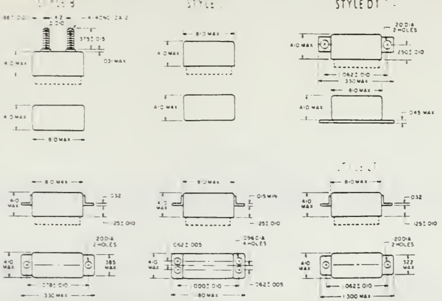
Switching times	4 milliseconds maximum at nominal coil voltage et 25 degrees C; the eddition of en arc-inhibiting diode across the coil will increase release time to 15 milliseconds meximum.
Life	100,000 operations with a 2-ampere contect loed.
Reliability	Designed to meet MIL-R-5757 (test results are aveilable).

ELECTRICAL CHARACTERISTICS:

Contect rating	2 emperes resistive, end 1 empere inductive (100 millijoules meximum stored inductive energy; time constent, 6 milliseconds). Contacts can withstand 4 amperes overload for 100 cycles without exceeding specified contact resistance. Available for low level switching.
Contact resistence	0.05 ohm maximum initially, 0.10 ohm maximum after rated life.
Dielectric strength	1000 volts rms, 500 volts between open contacts end between coil and cese, 350 volts between terminals at 80,000 feet.
Insuletion resistence	1000 megohms minimum (100 volts dc, 25 degrees C, 50 percent reletive humidity maximum).
Power requirement	220 milliwatts maximum at pull-in at 25 degrees C.

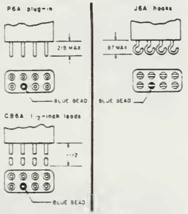
ENVIRONMENTAL SPECIFICATIONS:

Tempereture range	−65 to 125 degrees C.
Vibretion	30 g's from 5 to 3000 cps.
Shock	150 g's at 11 milliseconds.
Acceleration	Relay will operate while being subjected to a force of 100 g's along any axis.
General	Hermetic seal assures conformence with other environments such es fungus, sand and dust, humidity, eltitude, etc.



NOTE: DJS relays (arc-inhibited coils) require slightly higher housings: 0.550 inch maximum.

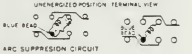
HEADER TERMINAL STYLES



COIL DATA

Coil Part No	Nominal Coil Voltage	Resistance (ohms ±10% at 25°C)	Maximum Pull-in Voltage At 25°C	Maximum Pull-in Voltage At 125°C	Max. Drop-Out Voltage At 25°C
6	6.3 vdc	42	3.2	4.4	1.6
12	12.6	210	6.8	9.3	3.4
26	26.5	700	13.5	18.0	6.8 – 38
32	32.0	1300	16.8	23.0	8.4

Series DJS **CIRCUIT DIAGRAMS** Series DJ



ORDERING INFORMATION

Modification Letter: add the letter "S" to specify a relay with an internal arc inhibiting circuit.
Coil Part Number: Obtain from Coil Data Table.
Relay Mounting Style: Refer to illustrated mounting styles.
Header Terminal Style: "J" signifies hooks. "P" signifies pins, and "AJ" signifies 1 1/2 inch leads. The number refers to the number of relay contacts (there are 6 in a 2pdt header). "A" is a contact code letter.
Low Level Testing Letter: "S" means that the relay is suitable for low-level switching applications and has received a low-level miss test (30 microamperes, 30 millivolts, and 100 ohms maximum).

DJ S 26 C1 P6A S

- RELAY SERIES LETTER
- MODIFICATION LETTER
- COIL PART NUMBER
- RELAY MOUNTING STYLE
- HEADER TERMINAL STYLE
- LOW-LEVEL TESTING LETTER
- DASH NUMBER (Deutsch Filtors' code for special relays)

EAST NORTHPORT, LONG ISLAND, NEW YORK 11731 / (516) 266-1600

APPENDIX H

ANALOG TO DIGITAL CONVERTER TECHNICAL DATA (HAS-1202)

ANALOG DEVICES

Ultra-Fast Hybrid Analog-to-Digital Converters

HAS-0802/1002/1202

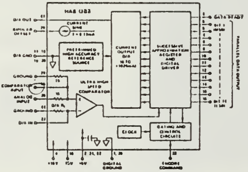
FEATURES

Conversion Times as Low as 1.2μs
Resolution: 8, 10 and 12 Bits
Exceptional Accuracy, 0.012% of F.S.
Low Power
Contained in Glass or Metal 32-Pin DIP
Adjustment-Free Operation

APPLICATIONS

Waveform Analysis
Fast Fourier Transforms
Radar

HAS-0802/1002/1202 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

With a typical conversion time of only 2.2μs for complete 12-bit conversion, the Analog Devices' HAS series hybrid A/D converters are among the fastest, smallest, most complete successive-approximation A/D's available. Housed in 32-pin DIP packages, these converters feature laser trimming for accuracy and linearity surpassing the best modular competitive A/D's. This series offers a unique combination of flexibility and simplicity which allows them to be used as stand-alone A/D converters requiring no additional external potentiometers and needing only an analog input signal and encode command for operation.

The HAS-1202 A/D features an accuracy of 0.012% and when combined with an HTC-0300 track-and-hold, forms an A/D conversion system capable of up to 350kHz sampling rates.

The HAS series A/D's are ideally suited for applications requiring excellent performance characteristics, small size, low power consumption and adjustment-free operation. Some of these applications include radar, PCM, data-acquisition, and digital-signal-processing systems where FFT's and other digital processing techniques are to be performed on analog input data.

Extreme care in circuit layout should be exercised when using these hybrids in order to obtain rated performance. In particular, input and output runs should be as short as possible, a ground plane should be used to tie all ground pins together, and power supplies should be bypassed as close to the hybrid circuit power supply pins as possible. Do not allow input or other analog signal lines to be in close proximity to or cross over any digital output line.

10

SPECIFICATIONS (typical @ +25°C with nominal voltages unless otherwise noted)

MODEL	UNITS	HAS-0801	HAS-1001	HAS-1185
RESOLUTION	BITS	8	10	12
LSB Weight	% Full Scale	0.4	0.1	0.035
	mV	40	10	2.5
RELATIVE ACCURACY (INCLUDING LINEARITY)	% Full Scale	0.05	0.051	0.015
Quantization Error	LSB	±1/2	*	*
LINEARITY VS. TEMPERATURE	ppm/°C	5 (No Missing Codes over Temperature Range)	*	*
INPUT OFFSET VOLTAGE				
Initial (Trimmable to Zero)	mV	10	*	*
Zero Offset vs. Temperature	μV/°C	15	*	*
Bipolar Offset vs. Temperature	μV/°C	100	*	*
GAIN ERROR				
Initial (Trimmable to Zero)	% Full Scale	0.1	*	*
Gain vs. Temperature	ppm/°C	50	*	*
INPUT				
Ranges (Full Scale)				
"Built-In" Standard Unipolar	V ±0.1%	+10.24	*	*
Bipolar	V ±0.01%	±5.12	*	*
Resistor Programmable (See Figure 5)	V, 0 nom	+5, +7.5, +15, +20, ±2.5, ±5.75, ±5.5, ±10		
Impedance	Ω min	1000	*	*
Overvoltage	V	Two Times Full Scale + or −		
CONVERSION TIME (COMPLETE CYCLE TIME)	μs max (typ)	1.5 (1.2)	1.7 (1.4)	3.0 (2.2)
CONVERSION RATE	kHz max	665	588	335
ENCODE COMMAND – TTL LOGIC INPUT				
Logic Levels (Positive Logic)	V	"0" = 0 to +0.4, "1" = +2 to +5		
Function[1]		Logic "1" Resets Converter; Logic "0" Starts Conversion		
Loading		1 Standard TTL Load: "0" = −1.6mA, max; "1" = 40μA, max		
Pulse Width	ns min	100	*	*
Repetition Rate		0 to Maximum Conversion Rate		
LOGIC OUTPUTS				
Data Ready ($\overline{DR}$) Function		Signals conversion is complete when low. After $\overline{DR}$ goes low, data is valid. A new conversion may be initiated at this time. $\overline{DR}$ may be used to strobe data into external register if adequate register setup time is allowed.		
Timing		See Figure 1		
Loading		5 Standard TTL Loads, max		
Parallel Data Format		8-, 10-, or 12-bits parallel data. Valid from time $\overline{DR}$ output goes low until 20ns after receipt of next encode command.		
Logic Levels		TTL Compatible: "0" = 0V to +0.4V; "1" = +2.4V to +5V		
Loading		Will drive up to 5 Standard TTL Loads or 2 TTL "S" or "H" Loads.		
Coding[2]		Offset Binary (BIN) for Unipolar Inputs: +10.24V = 1111....1; 0V = 0000....0. Offset Binary (OBN) for Bipolar Inputs: +5.15V = 1111....1; 0V = 0111....1; −5.15V = 0000....0		
POWER REQUIREMENTS				
+14.5V to +15.5V (+18V Absolute Max)	mA	40	*	*
−14.5V to −15.5V (−18V Absolute Max)	mA	15	*	*
+4.75V to +5.25V (+7V Absolute Max)	mA	200	*	*
TEMPERATURE RANGE				
Operating (Case)	°C	0 to +70	*	*
Storage	°C	−55 to +125	*	*
PACKAGE OPTION[3]		HY12A (ceramic package)	HY15C (metal package)	

NOTES

[1] After converter is reset, all other logic signals, including clock, are internally preserved.

[2] When HAS series A/D's are used with HTC-0300 track/hold, output coding is complementary binary (CBN) for unipolar inputs and complementary offset binary (COB) for bipolar inputs (see Table 1).

[3] See Section 19 for package outline information.

*Specifications same as model HAS-0801.

Specifications subject to change without notice.

*Table I. Output Coding**

SCALE	INPUT OF HTC-0300	INPUT OF HAS-1202	DIGITAL OUTPUT
UNIPOLAR OPERATION			
FS-1LSB	-10.2375V	+10.2375V	111111111111
3/4 FS	- 7.6800V	+ 7.6800V	110000000000
1/2 FS	- 5.1200V	+ 5.1200V	100000000000
1/4 FS	- 2.5600V	+ 2.5600V	010000000000
+1LSB	- 0.0025V	+ 0.0025V	000000000001
0	0.0000V	0.0000V	000000000000
BIPOLAR OPERATION			
+FS-1LSB	- 5.1175V	+ 5.1175V	111111111111
0	0.0000V	0.0000V	100000000000
-FS+1LSB	+ 5.1175V	- 5.1175V	000000000001
-FS	+ 5.1200V	- 5.1200V	000000000000

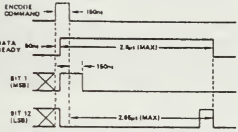
*Coding and input levels shown are for HAS-1202. For 8- and 10-bit A/D's the input levels are less by the values of the LSB weight for each type, and the digital output will show only 8 or 10 bits, respectively.

PIN DESIGNATIONS

HAS-1202*

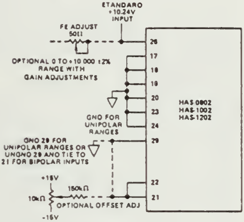
PIN	FUNCTION
1, 30	DIGITAL GROUND
2, 27, 31	+5V
3	DATA READY
4	+15V
5	BIT 1 OUTPUT (MSB)
6	BIT 2 OUTPUT
7	BIT 3 OUTPUT
8	BIT 4 OUTPUT
9	BIT 5 OUTPUT
10	BIT 6 OUTPUT
11	BIT 7 OUTPUT
12	BIT 8 OUTPUT
13	BIT 9 OUTPUT
14	BIT 10 OUTPUT
15	BIT 11 OUTPUT
16	BIT 12 OUTPUT (LSB)
17, 18, 19	ANALOG GROUND
20, 23, 24	ANALOG GROUND
21	D/A OUT
22	D/A IN
25	COMP INPUT
26	ANALOG INPUT
28	-15V
29	BIPOLAR OFFSET
32	ENCODE COMMAND

*HAS-1002, PINS 15 AND 16 ARE NOT CONNECTED INTERNALLY.
HAS-0802, PINS 13, 14, 15 AND 16 ARE NOT CONNECTED INTERNALLY.



TIMING SHOWN FOR HAS-1202. TIMING IS SIMILAR FOR HAS-1002 AND HAS-0802 EXCEPT LSB IS BIT 10 AND 8, RESPECTIVELY, AND TOTAL TYPICAL CONVERSION TIME IS 1.4µs AND 1.2µs, RESPECTIVELY.

Figure 1. Timing Diagram (Typical)



NOTES:
1. THIS CIRCUIT SHOWN FOR UNIPOLAR (0 TO +10.24V) INPUT. 0V INPUT = 000000000000; +10.24 INPUT = 111111111111.
2. FOR BIPOLAR (±5.12V) INPUT, UNGROUND PIN 29 AND CONNECT PIN 29 TO PIN 21.
3. FOR EXTRA-PRECISE GAIN (FULL-SCALE) ADJUSTMENT, CONNECT A 50Ω VARIABLE RESISTANCE IN SERIES WITH PIN 26 OF HAS-1202. THIS WILL RESULT IN 0 TO +10.000V INPUT WITH ADJUSTMENT RANGE OF ±2% OF FULL SCALE.
4. FOR EXTRA-PRECISE ZERO OFFSET ADJUSTMENT, CONNECT 150k RESISTOR FROM PIN 21 TO THE TAP OF A 10k POTENTIOMETER. END TERMINATIONS OF POTENTIOMETER CONNECT TO +15V AND -15V. THIS ZERO OFFSET ADJUSTMENT WILL HAVE A RANGE OF APPROXIMATELY ±100mV.

Figure 2. Input Connections For Standard Input Ranges

INPUT RANGE	R1	R2	Z_{IN}	ABSOLUTE MAXIMUM SIGNAL
0 to +5V, ±2.5V	SHORT	800	500	±10V
0 to +7.5V, ±3.75V	SHORT	2500	750	±15V
0 to +15V, ±7.5V	500	OPEN	1500	±30V
0 to +20V, ±10V	1000	OPEN	2000	±40V

Input Connections For Optional Input Ranges

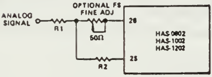


Figure 3. Full Scale Trim

APPLICATION CIRCUIT

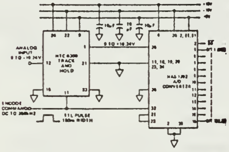


Figure 4. DC to 350kHz, 12-Bit, A/D Conversion System

ORDERING INFORMATION

Order model number HAS-0802, HAS-1002, or HAS-1202 for 8-, 10-, or 12-bit operation, respectively. Mating connector for the HAS series A/D's is model number HSA-2. Metal cased versions of this A/D with extended operating temperature range are also available. Consult the factory or nearest Analog Devices' sales office for further information.

APPENDIX I

FIFO TECHNICAL DATA (IDT 7201/SA)

Integrated Device Technology, Inc.

CMOS PARALLEL FIRST-IN/FIRST-OUT FIFO 256 x 9-BIT & 512 x 9-BIT

IDT 7200S/L
IDT 7201SA/LA

FEATURES:

- First-In/First-Out dual-port memory
- 256 X 9 organization (IDT7200)
- 512 x 9 organization (IDT7201A)
- Low power consumption
- Ultra high speed—35ns cycle time (28.5MHz)
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- IDT7200 and IDT7201A are pin and functionally compatible with Mostek MK4501, but with Half-Full Flag capability in single device mode
- Master/Slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning flags
- Auto retransmit capability
- High-performance CEMOS™ technology
- Available in plastic DIP, CERDIP, 300 mil THINDIP, LCC, PLCC and Flatpack
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-87531 is pending listing on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT7200/7201A are dual-port memories that utilize a special First-In/First-Out algorithm that loads and empties data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

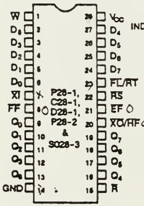
The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The devices have a read/write cycle time of 35ns (28.5MHz).

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

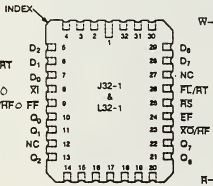
The IDT7200/1A are fabricated using IDT's high-speed CEMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

'N CONFIGURATIONS



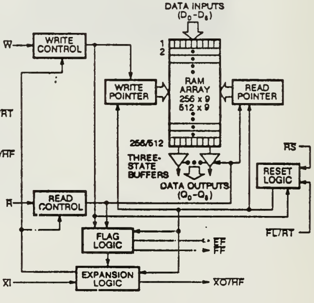
DIP/SOIC/FLATPACK TOP VIEW



LCC/PLCC TOP VIEW

CONSULT FACTORY FOR CERPACK PINOUT

FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} [1]	Input Low Voltage Commercial and Military	–	–	0.8	V

NOTE:

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7200S/L IDT7201SA/LA COMMERCIAL t_A = 25, 35ns			IDT7200S/L IDT7201SA/LA MILITARY t_A = 30, 40ns			IDT7200S/L IDT7201SA/LA COMMERCIAL t_A = 50, 65, 80, 120ns			IDT7200S/L IDT7201SA/LA MILITARY t_A = 50, 65, 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{LI} [1]	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	-1	–	1	-10	–	10	µA
I_{LO} [2]	Output Leakage Current	-10	–	10	-10	–	10	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = -2mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
I_{CC1} [3]	Active Power Supply Current	–	–	125[4]	–	–	140[4]	–	50	80	–	70	100	mA
I_{CC2} [3]	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}	–	–	15	–	–	20	–	5	8	–	8	15	mA
$I_{CC3}(L)$ [3]	Power Down Current (All Input = V_{CC} –0.2V)	–	–	500	–	–	900	–	–	500	–	–	900	µA
$I_{CC3}(S)$ [3]	Power Down Current (All Input = V_{CC} –0.2V)	–	–	5	–	–	9	–	–	5	–	–	9	mA

NOTES:

1. Measurements with $0.4 \leq V_{IN} \leq V_{CC}$.
2. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$
3. I_{CC} measurements are made with outputs open.
4. Tested at f = 20 MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L 7200x25 7201x25		MIL 7200x30 7201x30		COM'L 7200x35 7201x35		MIL 7200x40 7201x40		MILITARY AND COMMERCIAL 7200x50 7201x50		7200x65 7201x65		7201x80		7201x120		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_S	Shift Frequency	–	28.5	–	25	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{RC}	Read Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_A	Access Time	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	Read Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z (3)	5	–	5	–	5	–	5	–	10	–	10	–	10	–	10	–	ns
t_{WLZ}	Write Pulse Low to Data Bus at Low Z (3, 4)	5	–	5	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z (3)	–	15	–	20	–	20	–	25	–	30	–	30	–	30	–	35	ns
t_{WC}	Write Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	Write Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	15	–	18	–	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{RSC}	Reset Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	Reset Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	Reset Set-up Time	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
[illegible]	Retransmit Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	Retransmit Pulse Width (2)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTS}	Retransmit Set-up Time (3)	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{HFH}, t_{FFH}	Reset to Half-Full and Full Flag High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{REF}	Read Low to Empty Flag Low	–	25	–	30	–	30	–	30	–	45	–	60	–	60	–	60	ns
t_{RFF}	Read High to Full Flag High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WEF}	Write High to Empty Flag High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	25	–	30	–	30	–	35	–	45	–	30	–	60	–	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RHF}	Read High to Half-Full Flag High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{XI}	$\overline{XI}$ Pulse Width	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	–	15	–	15	–	15	–	15	–	15	–	15	–	15	–	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
lues guaranteed by design, not currently tested.
nly applies to read data flow-through mode.
5. "x" in part rating indicates power rating (S/SA or L/LA).

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is sampled and not 100% tested.

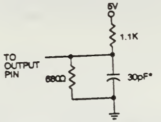


Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN (D_0–D_8)

Data inputs for 9-bit wide data.

CONTROLS

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the Read enable ($\overline{R}$) and Write enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read enable ($\overline{R}$) goes high, the Data Outputs (Q_0–Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7200/7201A can be made to retransmit data when the Retransmit enable control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read enable ($\overline{R}$) and Write enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 256/512 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go low after 256 writes for the IDT7200 and 512 writes for the IDT7201A.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

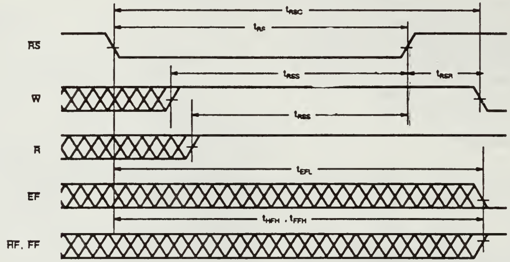
After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected Expansion Out ($\overline{XO}$) of the previous device. This output acts as a

signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q_0–Q_8)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.



NOTES:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
$\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of RS.

Figure 2. Reset

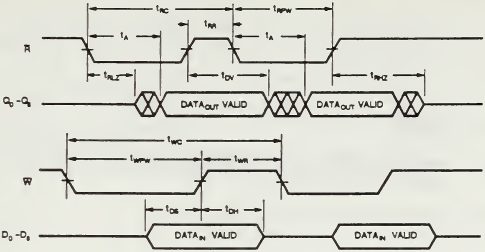


Figure 3. Asynchronous Write and Read Operation

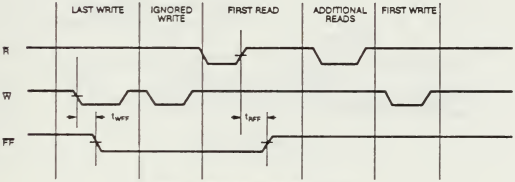


Figure 4. Full Flag From Last Write to First Read

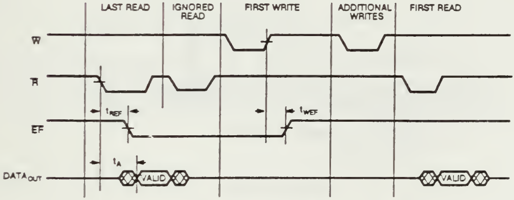
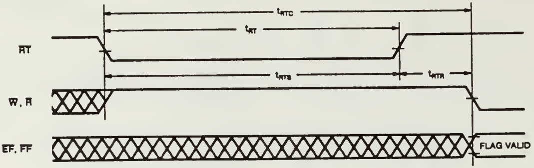


Figure 5. Empty Flag From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

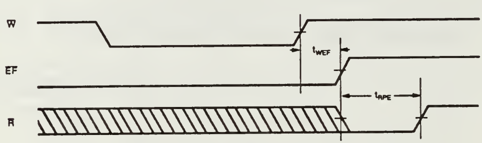


Figure 7. Empty Flag Timing

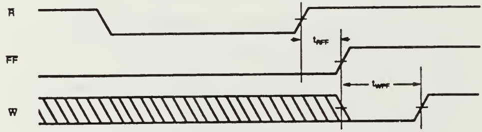


Figure 8. Full Flag Timing

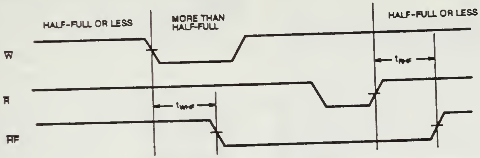


Figure 9. Half-Full Flag Timing

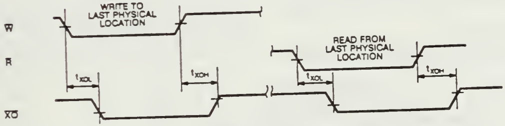


Figure 10. Expansion Out

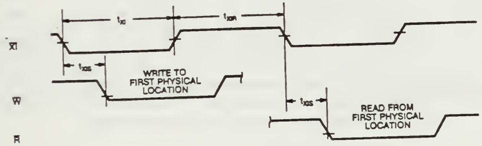


Figure 11. Expansion In

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7200/7201A may be used when the application requirements are for 256/512 words or less. The IDT7200/7201A is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12). In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

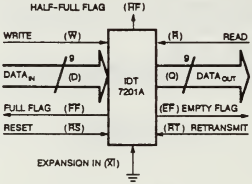
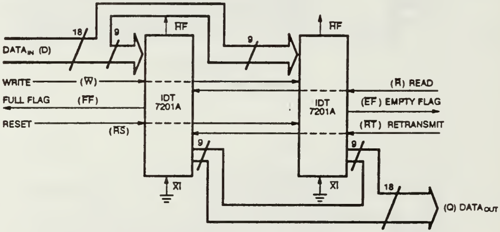


Figure 12. Block Diagram of Single 512x9 FIFO

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7201As. Any word width can be attained by adding additional IDT7201As.



NOTE:

1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$ and the $\overline{HF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 13. Block Diagram of 512x18 FIFO Memory Used in Width Expansion Mode

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7200/7201A can easily be adapted to applications where the requirements are for greater than 256/512 words. Figure 14 demonstrates Depth Expansion using three IDT7200/7201As. Any depth can be attained by adding additional IDT7200/7201As. The IDT7200/7201A operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7200/7201As as shown in Figure 16. Care must be taken to assure that the appropriate flag is monitored by each system, (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in (t_{WEF} + t_A)ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will de-assert the Empty Flag); however, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs."

TABLE I – RESET AND RETRANSMIT –

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X

NOTE:
1. Pointer will increment if flag is high.

TABLE II – RESET AND FIRST LOAD TRUTH TABLE –

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.

$\overline{RS}$ = Reset Input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

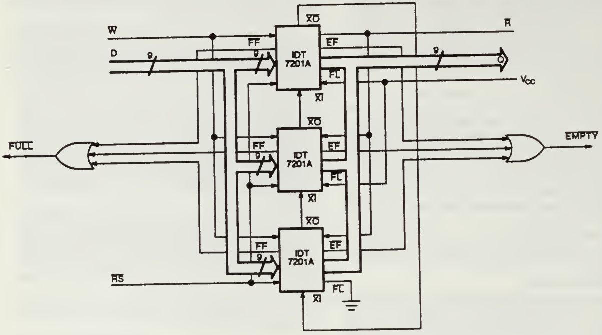
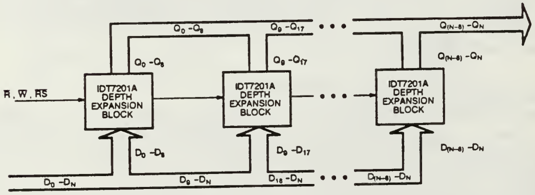


Figure 14. Block Diagram of 1536 x 9 FIFO Memory (Depth Expansion)



NOTES:

1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

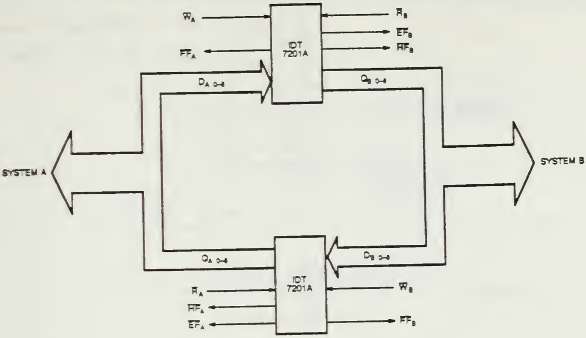


Figure 16. Bidirectional FIFO Mode

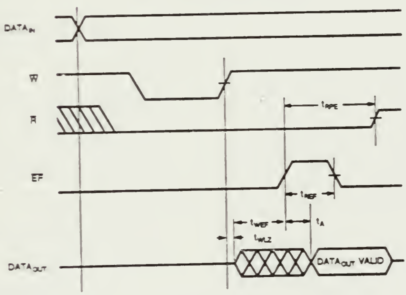


Figure 17. Read Data Flow-Through Mode

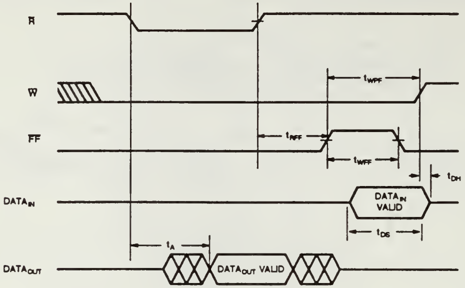


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT XXXX (Device Type) A (Power) 999 (Speed) A (Package) A (Process/Temperature Range)

Process/Temperature Range

Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

Package

SO	SOIC
P	Plastic Dip
D	CERDIP
TC	Sidebraze THINDIP
J	Plastic Leaded Chip Carrier
L	Leadless Chip Carrier
TP	Plastic THINDIP
XE	Cerpack

Speed — Access Time (t_A) Speed in Nanoseconds

25	Commercial Only
30	Military Only
35	Commercial Only
40	Military Only
50	
65	
80	
120	

Power

SA	Standard Power*
LA	Low Power*

Device Type

7200	256 x 9-Bit FIFO
7201	512 x 9-Bit FIFO

* "A" to be included for 7201 ordering part number only.

APPENDIX J

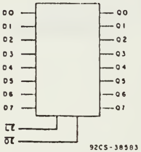
OCTAL LATCH TECHNICAL DATA (CD 54HC373)

Technical Data

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

File Number 1679

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Octal Transparent Latch, 3-State Output

Type Features:

- *Common latch enable control*
- *Common 3-state output enable control*
- *Buffered inputs*
- *3-State outputs*
- *Bus line driving capacity*
- *Typical propagation delay = 12 ns @ V_{CC} = 5V, C_L = 15 pF, T_A = 25° C (Data to Output for HC373)*

The RCA CD54/74HC373/573 and CD54/74HCT373/573 are high speed Octal Transparent Latches manufactured with silicon gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LSTTL devices. The CD54/74HCT373/573 are functionally as well as pin compatible with the standard 54/74LS373 and 573.

The outputs are transparent to the inputs when the latch enable ($\overline{LE}$) is high. When the latch enable ($\overline{LE}$) goes low the data is latched. The output enable ($\overline{OE}$) controls the 3-state outputs. When the output enable ($\overline{OE}$) is high the outputs are in the high impedance state. The latch operation is independent to the state of the output enable. The 373 and 573 are identical in function and differ only in their pinout arrangements.

The CD54HC/HCT373/573 are supplied in 20 lead ceramic dual-in-line packages (F suffix). The CD74HC/HCT373/573 are supplied in a 20-lead plastic dual-in-line plastic package (E suffix) and in 20-lead surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

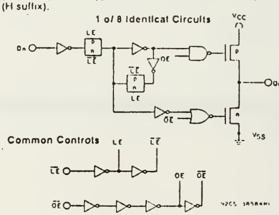


Fig. 1 - Logic diagram.

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  I_I ≤ 1 μA @ V_{OL}, V_{OH}

TRUTH TABLE

$\overline{\text{Output}}$ Enable	$\overline{\text{Latch}}$ Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

Note:
L = Low voltage level
H = High voltage level
X = Don't Care
Z = High Impedance State
l = Low voltage level one set-up time prior to the high to low latch enable transition
h = High voltage level one set-up time prior to the high to low latch enable transition

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

MAXIMUM RATINGS, *Absolute-Maximum Values.*

DC SUPPLY-VOLTAGE (V_{CC})
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR V_I < -0.5 V OR V_I > V_{CC} +0.5 V) .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR V_O < -0.5 V OR V_O > V_{CC} +0.5 V) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} +0.5 V) .... ±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}) .... ±70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 8 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC373, CD54/74HCT373
TERMINAL ASSIGNMENT

CD54/74HC573, CD54/74HCT573
TERMINAL ASSIGNMENT

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC373/CD54HC373 CD74HC573/CD54HC573 TEST CONDITIONS V_I V	I_O mA	V_{CC} V	74HC/54HC TYPE +25°C Min	Typ	Max	74HC TYPE -40/+85°C Min	Max	54HC TYPE -55/+125°C Min	Max	CD74HCT373/CD54HCT373 CD74HCT573/CD54HCT573 TEST CONDITIONS V_I V	V_{CC} V	74HCT/54HCT TYPE +25°C Min	Typ	Max	74HCT TYPE -40/+85°C Min	Max	54HCT TYPE -55/+125°C Min	Max	UNITS
High-Level Input Voltage V_{IH}			2	1.5	—		1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional Quiescent Device Current per Input Pin 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA
3-State Leakage Current	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS * HCT373	HCT573
$\overline{OE}$	1.5	1.25
Dn	0.4	0.3
LE	0.6	0.65

* Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 µA max. @ 25°C.

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay					
Data to Qn Output (HC/HCT373) (Fig. 3)	t_{PLH} t_{PHL}	15	12	13	ns
Data to Qn Output (HC/HCT573) (Fig. 3)	t_{PLH} t_{PHL}	15	14	17	ns
$\overline{LE}$ to Qn Output (Fig. 4)	t_{PLH} t_{PHL}	15	14	14	ns
Output Enabling Time (Fig. 6, 7)	t_{PZL} t_{PZH}	15	12	14	ns
Output Disabling Time (Fig. 6, 7)	t_{PLZ} t_{PHZ}	15	12	14	ns
Power Dissipation Capacitance (HC/HCT573, 373)	C_{PD}*	—	51	53	pF

*C_{PD} determines the no-load dynamic power consumption per latch. It is obtained by the following relationship:
P_D (total power per latch) = $V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency,
C_L = output load capacitance, V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

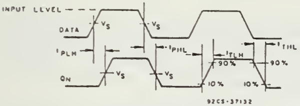
CHARACTERISTIC	TEST CONDITIONS V_{CC} V	LIMITS												UNITS
		25°C				-40°C to +85°C				-55°C to +125°C				
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{LE}$ Pulse Width t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
(Fig. 3)	4.5	16	—	16	—	20	—	20	—	24	—	24	—	ns
	6	14	—	—	—	17	—	—	—	20	—	—	—	
Set-up Time t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	
Data to $\overline{LE}$ 573	4.5	10	—	13	—	13	—	16	—	15	—	20	—	ns
(Fig. 4)	6	9	—	—	—	11	—	—	—	13	—	—	—	
Set-up Time t_{SU}	2	50	—	—	—	65	—	—	—	75	—	—	—	
Data to $\overline{LE}$ 373	4.5	10	—	13	—	13	—	16	—	15	—	20	—	ns
(Fig. 4)	6	9	—	—	—	11	—	—	—	13	—	—	—	
Hold Time t_H	2	40	—	—	—	50	—	—	—	60	—	—	—	
Data to $\overline{LE}$ 573	4.5	8	—	10	—	10	—	13	—	12	—	15	—	ns
(Fig. 4)	6	7	—	—	—	9	—	—	—	10	—	—	—	
Hold Time t_H	2	5	—	—	—	5	—	—	—	5	—	—	—	
Data to $\overline{LE}$ 373	4.5	5	—	10	—	5	—	13	—	5	—	15	—	ns
(Fig. 4)	6	5	—	—	—	5	—	—	—	5	—	—	—	

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573

SWITCHING CHARACTERISTICS (Input t_r, t_f = 6 ns, C_L = 50 pF)

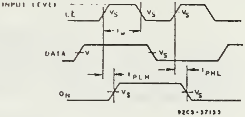
CHARACTERISTIC	TEST CONDITIONS V_{CC} V	LIMITS 25°C HC Min.	Max.	HCT Min.	Max.	-40°C to +85°C 74HC Min.	Max.	74HCT Min.	Max.	-55°C to +125°C 54HC Min.	Max.	54HCT Min.	Max.	UNITS
Propagation Delay t_{PLH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Data to Qn t_{PHL}	4.5	—	30	—	32	—	38	—	40	—	45	—	48	ns
(Fig. 2) HC/HCT373	6	—	26	—	—	—	33	—	—	—	38	—	—	
Data to Qn t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
(Fig. 2) t_{PHL}	4.5	—	35	—	40	—	44	—	50	—	53	—	60	ns
HC/HCT573	6	—	30	—	—	—	37	—	—	—	45	—	—	
$\overline{LE}$ to Qn t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	
t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	ns
(Fig. 3)	6	—	30	—	—	—	37	—	—	—	45	—	—	
Output Enabling t_{PZL}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Time t_{PZH}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
(Figs. 5 & 6)	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Disabling t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Time t_{PHZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
(Figs. 5 & 6)	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
(Fig. 2)	6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance C_O	—	—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC373, CD54/74HCT373
CD54/74HC573, CD54/74HCT573



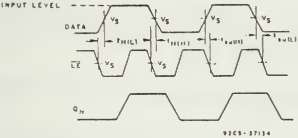
	54/74HC	54/74HCT
Input Level	Vcc	3 V
V_s	50% Vcc	1.3 V

Fig 2 - Data to Q_n output propagation delays and output transition times.



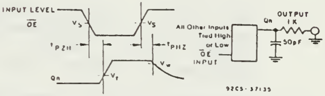
	54/74HC	54/74HCT
Input Level	Vcc	3 V
V_s	50% Vcc	1.3 V

Fig. 3 - Latch enable propagation delays.



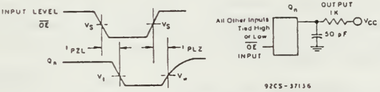
	54/74HC	54/74HCT
Input Level	Vcc	3 V
V_s	50% Vcc	1.3 V

Fig 4 - Latch enable prerequisite times.



	54/74HC	54/74HCT
Input Level	Vcc	3 V
V_s	50% Vcc	1.3 V
V_i	50% Vcc	1.3 V
V_o	90% Vcc	90% Vcc

Fig 5 - Three-state propagation delays.



	54/74HC	54/74HCT
Input Level	Vcc	3 V
V_s	50% Vcc	1.3 V
V_i	50% Vcc	1.3 V
V_o	10% Vcc	10% Vcc

Fig. 6 - Three-state propagation delays.

LIST OF REFERENCES

1. Cleary, D. D., "A Sounding Rocket Experiment For Remote Sensing The Ionosphere E- And F-Layers," Proposal submitted to the Office of Naval Research, Naval Postgraduate School, Monterey, California, August 1989.

2. Naval Research Laboratory, Drawing Number H1-M-1, **HIRAAS/MUSTANG Rocket Payload,** by B. McAllister, August 1989.

3. Goddard Space Flight Center, NASA Reference Publication 1171 **Pulse Code Modulation (PCM) Encoder Handbook for Aydin Vector MMP-600 Series System**, by S. F. Currier and W. R. Powell, 1986.

4. Memo from Instrumentation Engineer, NASA (Wallops Island), to Payload Manager, Subject: Instrumentation System Design Review Package for Payload 36.053 McCoy/Naval Research Lab, 5 June 1989.

5. Hamamatsu, SD-03, **Characteristics and Use of PCD Linear Image Sensors,** Hamamatsu, 1987.

6. Research Support Instruments, Drawing Number 15-267-0-40, **Spectrograph and Telescope Interface,** by M. Yaker, 23 June 1989.

7. Electro-Optical Products Division, ITT, F4145, **Proximity Focused Channel Intensifier Tubes With Dual Microchannel Plates,** June 1986.

8. Electrical Systems Engineer--NASA (Wallops Island), to Payload Manager, Subject: Design Review for Terrier Black Brant 36.053 (McCoy/Naval Research Laboratory/White Sands Missile Range/February 1990), 15 August 1989.

9. Conversation between Dr. David D. Cleary, Professor Naval Postgraduate School, Monterey, California, October 1989.

10. Naval Research Laboratory, Drawing Number H-1027, **MUSTANG WIRING,** by H. Merchant, 19 July 1989.

11. Naval Research Laboratory, Drawing Number H-1022, **MUSTANG WIRING,** by H. Merchant, 19 July 1989.

12. Barnes, J. R., **Electronic System Design: Interference and Noise Control Techniques,** pp. 1-119, Prentice-Hall, Inc., 1987.

INITIAL DISTRIBUTION LIST

		No. Copies
1.	Defense Technical Information Center Cameron Station Alexandria, Virginia 22304-6145	2
2.	Library, Code 0142 Naval Postgraduate School Monterey, California 93943-5002	2
3.	Chairman, Code 62 Department of Electrical and Computer Engineering, Naval Postgraduate School Monterey, California 93943-5000	1
4.	Space Systems Academic Group, Code 72 Naval Postgraduate School Monterey, California 93943-5100	1
5.	Prof. Sherif Michael, Code 62Mi Department of Electrical and Computer Engineering Naval Postgraduate School Monterey, California 93943-5000	1
6.	Prof. David Cleary, Code 61Cl Department of Physics Naval Postgraduate School Monterey, California 93943-5000	4
7.	Lieutenant Richard S. Campbell 885 Doris Drive Arnold, Maryland 21012	2

Thesis
C19386 Campbell
c.1 Development and integration of the NPS middle ultraviolet spectrograph with an extreme ultraviolet spectrograph.